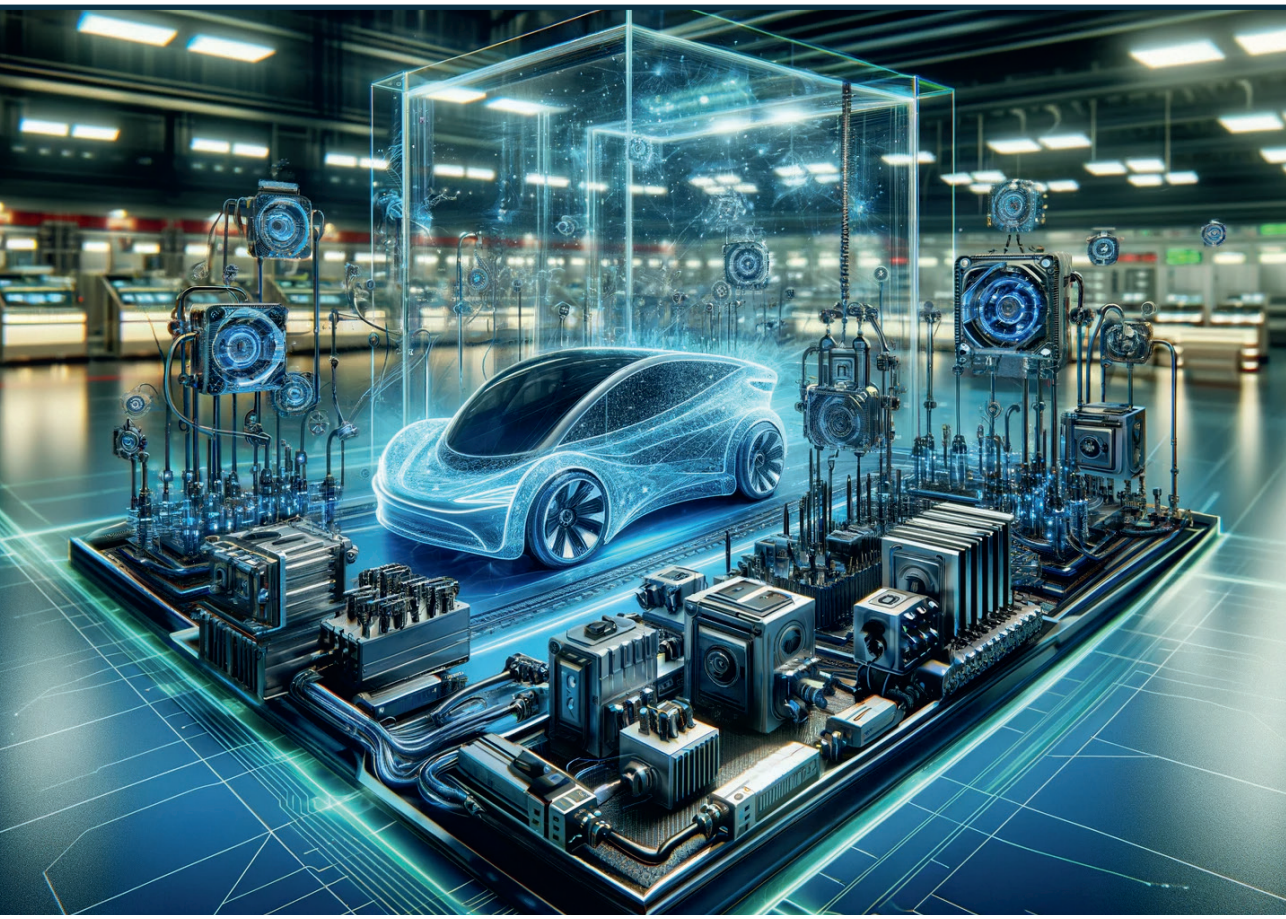
RIGA TECHNICAL UNIVERSITY

Artūrs Bogdanovs

RESEARCH AND DEVELOPMENT OF AUXILIARY CONVERTERS FOR APPLICATION IN ELECTRIC VEHICLES

Doctoral Thesis



RTU Press
Riga 2023

RIGA TECHNICAL UNIVERSITY
Faculty of Electrical and Environmental Engineering
Institute of Industrial Electronics and Electrical Engineering

Artūrs Bogdanovs

Doctoral Student of the Study Programme "Computerised Control of Electrical Technologies"

RESEARCH AND DEVELOPMENT OF AUXILIARY CONVERTERS FOR APPLICATION IN ELECTRIC VEHICLES

Doctoral Thesis

Scientific supervisor
Professor Dr. sc. ing.
OSKARS KRIEVS

Scientific advisor
Professor Dr.
JOHANNES PFORR

RTU Press
Riga 2023

Bogdanovs, A. Research and Development of Auxiliary Converters for Application in Electric Vehicles. Doctoral Thesis. Riga: RTU Press, 2023. 85 p.

Published in accordance with the decision of the Promotion Council "P-14" of 23 October 2023, Minutes No. 04030-9.12.2/7.

This work has been supported by the European Social Fund within the Project No 8.2.2.0/20/I/008 «Strengthening of PhD students and academic personnel of Riga Technical University and BA School of Business and Finance in the strategic fields of specialization» of the Specific Objective 8.2.2 «To Strengthen Academic Staff of Higher Education Institutions in Strategic Specialization Areas» of the Operational Programme «Growth and Employment»

This research/publication was supported by Riga Technical University's Doctoral Grant programme.

DOCTORAL THESIS PROPOSED TO RIGA TECHNICAL UNIVERSITY FOR THE PROMOTION TO THE SCIENTIFIC DEGREE OF DOCTOR OF SCIENCE

To be granted the scientific degree of Doctor of Science (Ph. D.), the present Doctoral Thesis has been submitted for defence at the open meeting of RTU Promotion Council on 29 December 2023 13.30 at the Faculty of Electrical and Environmental Engineering of Riga Technical University, Azenes Street 12/1, Room 212.

OFFICIAL REVIEWERS

Assoc. Professor Dr. sc. ing. Jānis Zaķis
Riga Technical University

Senior Researcher Ph. D. Dmitri Vinnikov
Tallinn University of Technology, Estonia

Professor Ph. D. Sonata Tolvaišiene
Vilnius Gediminas technical university, Lithuania

DECLARATION OF ACADEMIC INTEGRITY

I hereby declare that the Doctoral Thesis submitted for review to Riga Technical University for promotion to the scientific degree of Doctor of Science (Ph. D.) is my own. I confirm that this Doctoral Thesis has not been submitted to any other university for the promotion to a scientific degree.

Artūrs Bogdanovs ……. (signature)
Date: ……

The Doctoral Thesis has been written in English. It consists of an Introduction, 4 chapters, Conclusions, 66 figures, and 6 tables; the total number of pages is 85. The Bibliography contains 75 titles.

ABSTRACT

The Doctoral Thesis is titled “Research and Development of Auxiliary Converters for Application in Electric Vehicles.” The aim of the Thesis is to research and develop an energetically and economically effective technology for auxiliary converter systems in electric vehicles, in accordance with the actual industry needs, as well as to create a scientific contribution and disseminate the acquired knowledge by introducing new concepts in the proposed converter design. The main research object of the Thesis is the auxiliary converter system, consisting of non-isolated DC/DC converters and DC/AC inverters for auxiliary drives. The main research methods include the determination of the appropriate auxiliary converter topologies, adjusting the converter mathematical model parameters, developing simulation models, and evaluating the results of simulations, developing auxiliary converter prototypes and performing experimental verification in a laboratory environment. The main research results cover a set of recommendations and technological improvements for the practical application in the auxiliary converter systems of electric vehicles. The total energy savings by auxiliaries in electric vehicles can reach up to 10 % with stress reduction by up to 80 % and considerable functionality improvements in reliability and fault tolerance.

Chapter 1 deals with the investigation and development of novel current sensing and measurement techniques in auxiliary converters. The novel indirect current measurement technique allows to achieve a cost-efficient auxiliary converter sensing and measurement design with functionality of the current sensing and balancing with adequate accuracy and measurement errors below 0.5 A resulting in no efficiency degradation; fault detection and identification; as well as the fault-tolerant operation. In chapter 2 a detailed coupled inductor analysis is performed and the fuzzy logic current balancing and output voltage regulation controller with optimized steady-state and dynamic performance has been developed. Chapter 3 describes the indirect current sensing-based fault detection and the concept of fault tolerant operation. Implementation results have shown fast fault detection and identification capability within 1 converter switching period or 20 µs and efficient fault-tolerant operation that can allow converter operation with active fault condition and improve efficiency by up to 2 %, at the same time ensuring fail safe and reliable converter operation for the safety critical systems. Chapter 4 is dedicated to the energy efficiency topic in auxiliary converters. Wide bandgap semiconductor utilization and auxiliary drive design with permanently excited synchronous machine and multi-level inverter utilizing modern GaN devices ensures energy savings by up to 10 %, more reliable faster operation with thermal and mechanical stress reduction up to 80 % and is economically effective solution in scope of the whole converter’s life cycle in electric vehicle operation.

The Doctoral Thesis is written in English. It consists of an Introduction; 4 Chapters; Conclusions; 66 figures; 6 tables; the total number of pages is 85; the References contains 75 titles.

ANOTĀCIJA

Promocijas darba nosaukums ir "Pašpatēriņa pārveidotāju izpēte un izstrāde elektrotransporta vajadzībām." Promocijas darba mērķis ir izpētīt un attīstīt enerģētiski un ekonomiski efektīvu tehnoloģiju elektrisko transportlīdzekļu pašpatēriņa pārveidotāju sistēmām, atbilstoši aktuālajām industrijas vajadzībām, kā arī radīt zinātnisku pienesumu un izplatīt iegūtās zināšanas, ieviešot jaunas koncepcijas piedāvāto pārveidotāju konstrukcijā. Promocijas darba galvenais izpētes objekts ir pašpatēriņa pārveidotāju sistēma, kas sastāv no neizolētiem DC/DC līdzstrāvas pārveidotājiem un DC/AC invertoriem pašpatēriņa sistēmu piedziņai. Galvenās pētniecības metodes ietver atbilstošu pašpatēriņa pārveidotāju topoloģiju identificēšanu, pārveidotāja matemātiskā modeļa parametru pielāgošanu, simulācijas modeļu izstrādi un simulāciju rezultātu novērtēšanu, pašpatēriņa pārveidotāju prototipu izstrādi un eksperimentālās verifikācijas veikšanu laboratorijas vidē. Galvenie pētījumu rezultāti aptver ieteikumu un tehnoloģisko uzlabojumu kopumu praktiskai pielietošanai elektrisko transportlīdzekļu pašpatēriņa pārveidotāju sistēmās. Kopējais enerģijas ietaupījums, ko piedāvātie risinājumi rada pašpatēriņa sistēmā elektriskajos transportlīdzekļos, var sasniegt līdz pat 10 %, samazinot termomehāniskās slodzes līdz pat 80 % un ievērojami uzlabojot uzticamības funkcionalitāti un bojājumpiecietību.

1. nodaļā aplūkota jaunu strāvas sensoru un mērīšanas metožu izpēte un izstrāde pielietošanai pašpatēriņa pārveidotājos. Jaunā netiešās strāvas mērīšanas metode ļauj panākt rentablu papildu pārveidotāja sensoru dizainu un mērījumu metodiku ar strāvas noteikšanas un balansēšanas funkcionalitāti ar atbilstošu precizitāti un mērījumu kļūdām zem 0,5 A bez veiktspējas samazinājuma; defektu noteikšanu un identificēšanu; kā arī bojājumpiecietīgu darbību. 2. nodaļā ir sagatavota detalizēta magnētiski saistītu indukcijas spoļu analīze un izstrādāts izplūdušās loģikas strāvas balansēšanas un izejas sprieguma regulēšanas kontrolieris ar optimizētu stacionāra režīma un dinamisku veiktspēju. 3. nodaļā aprakstīta uz netiešo strāvu mērījumiem balstīta bojājumu noteikšana un bojājumpiecietīgas darbības nodrošināšana. Rezultāti ir parādījuši ātru kļūdu noteikšanas un diagnostikas spēju 1 pārveidotāja pārslēgšanās perioda jeb 20 μs laikā un efektīvu bojājumpiecietīgu darbību, kas var ļaut pārveidotājam darboties aktīva bojājuma apstākļos un uzlabot efektivitāti līdz pat 2 %, vienlaikus nodrošinot bezatteikumu un uzticamu pārveidotāju darbību drošības kritisku sistēmu gadījumā. 4. nodaļa ir veltīta energoefektivitātes tēmai pašpatēriņa pārveidotājos. Platjoslas pusvadītāju izmantošana un pašpatēriņa piedziņas sistēmu dizains ar pastāvīgo magnētu ierosmes sinhrono mašīnu un daudzlīmeņu invertoru, izmantojot modernos GaN pusvadītājus, nodrošina enerģijas ietaupījumu līdz pat 10 %, ātrdarbību un drošumu ar termisko un mehānisko slodžu samazinājumu līdz 80 %, kā arī ekonomiski efektīvu risinājumu pilnā elektrotransporta pārveidotāju dzīves cikla laikā.

Promocijas darbs ir uzrakstīts angļu valodā. Tas sastāv no ievada; 4 nodaļām; secinājumiem; 66 attēliem; 6 tabulām; kopējais lappušu skaits ir 85; literatūras sarakstā ir 75 atsauces.

ACKNOWLEDGEMENTS

Firstly, I would like to express my gratitude to my scientific supervisor prof. Dr. Oskars Krievs for his endless support, valuable comments, and always positive attitude throughout my whole PhD project.

Secondly, I would like to show my appreciation to my adviser prof. Dr. Johannes Pforr for introducing me to the wonderful world of power electronics, advising me in professional growth as a scientist, guiding and steering me in the right direction always when it was required despite all the circumstances. His valuable "Anmerkungen" always promoted deeper analysis of investigated topics, view from different perspectives and preparation of high-quality publications.

I would like to acknowledge all co-authors of publications and especially prof. Leonīds Ribickis, prof. Ilya Galkin and asoc. prof. Laila Zemīte for their significant contribution to my scientific skill development.

I would like to thank all my colleagues in the Institute of Industrial Electronics and Electrical Engineering and especially to Aleksander Bubovich, Kristaps Vītols, and Pavels Suskis for providing me with useful tips for experiments and their trustful support. Special thanks for the Faculty of Electrical and Environmental Engineering administrator Mr. Aleksandras Dimitrovas for his emotional and organizational support!

I would like to acknowledge colleagues from Institute of Transport and Department of Automotive Engineering for their feedback and providing me an opportunity to do teaching assistance and contribution to my professional growth as a lecturer.

I would like to express my acknowledgements to this Thesis reviewers for their engagement and valuable feedback.

Finally, I would like to thank all my friends and family for their understanding, encouragement, and support in difficult times.

CONTENTS

GENERAL OVERVIEW OF THE THESIS

Motivation and Background

Transport sector makes about a quarter of total greenhouse gas emissions in Europe and is, therefore, the main contributor to the climate change currently. To significantly reduce the environmental footprint, the European Commission has stated a goal to reduce the greenhouse gas emissions in transport sector by 90 % before 2050. To fulfil this goal, the most effective solution nowadays is transport sector transition towards electrified drivetrain technology. The number of electric vehicles has shown a gradual increase within the last decade and this number is expected to show a rapid growth in the future. This arises a lot of concerns regarding the vehicle energy consumption and efficiency.

The vehicle energy consumption consists of the energy drawn by the main propulsion (drive) system and auxiliary power required for the rest of the systems, located in a vehicle, e.g. lighting, signalling, control, pneumatic and hydraulic systems for steering and braking systems, heating, ventilation and air conditioning (HVAC). In the case of electric vehicles all the auxiliary systems must be supplied from the vehicle electrical energy net and, hence, the demand for auxiliary converter power in transportation applications continues to increase. In addition, more safety and comfort systems are being introduced that demands additional auxiliary power and results in increasing dimensions and weight of auxiliary converter systems.

Some vehicle auxiliary components, like power steering and braking system, are safety critical, i.e. there are catastrophic consequences in case of failure. Therefore, the fault-tolerance and reliability of auxiliary converter systems becomes crucial aspect and there is a demand for reliable solutions for auxiliary converters. As the component redundancy and the growing power consumption leads to increasing volume and weight, it results in the increased overall vehicle energy consumption. Hence, there is a need of cheap, reliable, energy efficient and environmentally friendly solutions in electric vehicle auxiliary converter design. However, the most of scientific contributions and research results are mainly focused on the advancements in the vehicle main drive systems, while the auxiliary converter systems are often neglected and are not in the top of current research interests, despite the growing industry demands and electric vehicle market potentials for growth.

Hypothesis and thesis for defence

1. Converter's voltage and current waveforms contain sufficient information about converter status that in combination with intelligent sensing can be utilized by control system to ensure improved fault tolerance and more reliable power supply thus increasing safety in critical auxiliary systems of electric vehicles.
2. Intelligent sensing and converter control systems with integrated status monitoring ensure operation with highest possible efficiency and optimized performance, even in an active failure mode by ensuring fast transition to the fault-tolerant operation mode and improving efficiency by ap to 2%.

3. Auxiliary drive design with permanently excited synchronous machine and multi-level inverter utilizing modern wide bandgap semiconductor devices ensures energy savings by 10%, more reliable faster operation and is economically effective solution in scope of the whole converter's life cycle in electric vehicle operation.

Research aim and objectives

The aim of the Thesis is to research and develop an energetically and economically effective technology for auxiliary converter systems in electric vehicles, in accordance with the actual industry needs, as well as to create a scientific contribution and disseminate the acquired knowledge by introducing new concepts in the proposed converter design.

The main objectives of the Thesis are:

1. To investigate and develop novel current sensing and measurement techniques in auxiliary converters.
2. To investigate and develop the control methods and to analyse the control performance under unpredictable auxiliary converter load conditions.
3. To develop a solution for the fault detection and to investigate the fault tolerant operation capabilities.
4. To analyse the wide bandgap semiconductor device application in auxiliary converters, including the cost vs benefit analysis.
5. To investigate and propose the solution for reliable and energy saving auxiliary drive operation.

Research object and scope

The main research object of the Thesis is the auxiliary converter system, consisting of non-isolated DC/DC converters and DC/AC inverters for auxiliary drives. The main scope of application is mainly focussed on different types of grid-connected electric vehicles and transportation, i.e. trolleybuses, trams and electric motorized units in light and heavy railways, as well as the battery electric vehicles. The proposed concepts and technological improvements may be applied in any type of vehicle auxiliary converter systems in whole or in part, however, the preliminary technology adaptation for the specific vehicle type is always required. The proposed indirect current sensing solution, fault detection and identification technique and the fault-tolerant operation algorithms can be used in any application, where the DC/DC or DC/AC multiphase or multilevel power converters are utilized.

Research tools and methods

To fulfil the aim of the Thesis, the incremental research design method is being used. The research stages include the determination of the appropriate auxiliary converter topologies, adjusting the converter mathematical model parameters, developing simulation models, and evaluating the results of simulations, developing auxiliary converter prototypes and performing

experimental verification in a laboratory environment. The prototypes of a 5-phase bi-directional DC/DC converter with coupled inductors and a 3-phase 3-level DC/AC inverter have been built for the proposed concepts and technological improvements validation in a laboratory environment. Hence, the research results correspond to the Technology Readiness Level 4 (TRL4).

Scientific novelty

1. Novel Indirect Current Measurement (ICM) technique, including voltage and current sensing circuit part and phase current reconstruction signal processing part, has been developed and integrated into the DC/DC converter and DC-AC inverter.
2. Fuzzy logic current balancing and output voltage regulation controller with optimized steady-state and dynamic performance has been developed based on the ICM and applied for the DC/DC converter control.
3. The common fault detection and identification method with fast response based on the extended signal processing of ICM has been developed and integrated into the DC/DC converter self-diagnosis system.
4. Fault-tolerant operation algorithm for the multiphase converter with strongly coupled inductors and small reaction time has been developed for reliable power supply to the safety critical systems.
5. A comparative analysis of the modern wide bandgap SiC and GaN semiconductor application in high voltage auxiliary converters is performed, including the evaluations of costs and benefits within the life cycle of converter.
6. An energy efficient and reliable auxiliary drive concept has been proposed and assessed by means of the case study on a vehicular air compressor example.

Practical relevance

The research results cover a set of recommendations and technological improvements for the practical application in the auxiliary converter systems of electric vehicles. The outcome of this work corresponds well with the industry demand for cheap, reliable, energy efficient and environmentally friendly solutions in electric vehicle auxiliary converter design requirements. The proposed concepts have been validated experimentally in the laboratory environment and, hence, can be further developed for the testing in the application relevant environment, certification, type approval and release to the market within the next 4 years.

In scope of the commercialization training program for scientists CO.LAB, the commercialization potential of the Thesis results has been assessed. As the result a technology road map has been created, total addressable market and market opportunities were evaluated, and the first version of business model has been developed for advancing the technology in the market in collaboration with industry partner JSC Riga Electric Machine Building Works.

Approbation of research results

14 publications were created in total, with 11 publications being presented in the Doctoral Thesis. The approbation and practical relevance of the research results is covered in the following publications:

1. Kondratieva, L., **Bogdanovs, A.**, Overianova, L., Riabov, I., Goolak, S. Determination of the Working Energy Capacity of the On-Board Energy Storage System of an Electric Locomotive for Quarry Railway Transport during Working with a Limitation of Consumed Power. *Archives of Transport*, 2023, Vol. 65, No. 1, pp. 119-136. ISSN 0866-9546. e-ISSN 2300-8830. Available from: doi:10.5604/01.3001.0016.2631
2. **Bogdanovs, A.**, Krievs, O., Pforr, J. Wide Bandgap SiC and GaN Semiconductor Performance Evaluation in a 3-Phase 3-Level NPC Inverter for Transportation Application. In: *2022 IEEE 63rd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2022): Conference Proceedings*, Latvia, Riga, 10-12 October, 2022. Piscataway: IEEE, 2022, pp.301-307. ISBN 978-1-6654-6559-5. e-ISBN 978-1-6654-6558-8. Available from: doi:10.1109/RTUCON56726.2022.9978767
3. Klints, A., **Bogdanovs, A.**, Zarembo, J. FEA Based Traction Converter Thermal Design Method for Railway Application Using Mission Profile Definition. In: *2022 IEEE 63rd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2022): Conference Proceedings*, Latvia, Riga, 10-12 October, 2022. Piscataway: IEEE, 2022, pp.74-80. ISBN 978-1-6654-6559-5. e-ISBN 978-1-6654-6558-8. Available from: doi:10.1109/RTUCON56726.2022.9978854
4. **Bogdanovs, A.**, Vonda, Ē., Grīslis, A., Gailis, M., Zalcmanis, G., Kreicbergs, J. E-Mobility Courses Design for Automotive Engineering Curricula: a Case Study. In: *2022 IEEE 63rd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2022): Conference Proceedings*, Latvia, Riga, 10-12 October, 2022. Piscataway: IEEE, 2022, pp.7-12. ISBN 978-1-6654-6559-5. e-ISBN 978-1-6654-6558-8. Available from: doi:10.1109/RTUCON56726.2022.9978797
5. **Bogdanovs, A.**, Bubovich, A., Galkin, I. Interdisciplinary Project-based Learning Approach Implementation for Undergraduate Electrical Engineering Students. In: *IEEE 63rd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2022): Conference Proceedings*, Latvia, Riga, 10-12 October, 2022. Piscataway: IEEE, 2022, pp.116-122. ISBN 978-1-6654-6559-5. e-ISBN 978-1-6654-6558-8. Available from: doi:10.1109/RTUCON56726.2022.9978862
6. **Bogdanovs, A.**, Krievs, O., Pforr, J. Fault-Tolerant Operation Algorithm for a Multi-Phase DC Converter with Coupled Inductors. In: *PCIM Europe Proceedings*, Germany, Nuremberg, 10-12 May, 2022. Berlin; Offenbach: VDE VERLAG

GMBH, 2022, pp.506-515. ISBN 978-3-8007-5822-7. Available from: doi:10.30420/565822070

7. **Bogdanovs, A.**, Krievs, O., Pforr, J. Fault Detection using Indirect DC Link Current Measurement Technique in Multiphase DC Converter with Coupled Inductor. In: *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe): Conference Proceedings*, Belgium, Ghent, 6-10 September, 2021. Piscataway: IEEE, 2021, pp.2890-2899. ISBN 978-1-6654-3384-6. e-ISBN 978-9-0758-1537-5.
8. **Bogdanovs, A.**, Kucajevs, J., Steiks, I., Vītols, K., Zemīte, L., Krievs, O., Leibčs, R. Opportunity Analysis of Battery Electric Vehicle Fast Charging Infrastructure Development in Latvia. In: *2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2021): Conference Proceedings*, Latvia, Riga, 15-17 November, 2021. Piscataway: IEEE, 2021, pp.324-331. ISBN 978-1-6654-3805-6. e-ISBN 978-1-6654-3804-9. Available from: doi:10.1109/RTUCON53541.2021.9711718
9. **Bogdanovs, A.**, Krievs, O., Pforr, J. Indirect Multiple DC Link Current Sensing Using Op-Amp Circuits in a Three-Phase Three-Level PWM Inverter. In: *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management: Proceedings. Vol.1*, Germany, Nuremberg, 3-7 May, 2021. Berlin; Offenbach: Mesago PCIM GmbH, 2021, pp.1614-1621. ISBN 978-3-8007-5515-8.
10. **Bogdanovs, A.**, Krievs, O., Ribickis, L., Pforr, J. Fuzzy Logic Current Balancing Controller Implementation in an Automotive Multi-Phase DC Converter with Coupled Inductors. In: *2020 IEEE 61st International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2020): Conference Proceedings*, Latvia, Riga, 5-7 November, 2020. Piscataway: IEEE, 2020, Article number 9316473. ISBN 978-1-7281-9511-7. e-ISBN 978-1-7281-9510-0. Available from: doi:10.1109/RTUCON51174.2020.9316473
11. **Bogdanovs, A.**, Krievs, O., Pforr, J. Indirect DC Link Current Measurement Technique Using an Op-Amp Circuit in an Automotive DC Converter with Coupled Inductors. In: International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management: Proceedings. Vol.1, Germany, Nuremberg, 7-8 July, 2020. Berlin; Offenbach: Mesago PCIM GmbH, 2020, pp.60-67. ISBN 978-3-8007-5245-4. ISSN 2191-3358.

INTRODUCTION

The demand for auxiliary converter power in transportation applications is increasing and this requires more complex solutions and novel approaches for auxiliary power supply design. As discussed in [1], the drawn auxiliary system power in trolleybuses has become so high that it is challenging to provide acceptable supply during momentary power interruptions due to travelling through insulated grid sections. A typical trolleybus electric power circuit functional diagram is shown in (Fig. 1) [2]. Another example is an electric locomotive power circuit functional diagram, depicted in (Fig. 2) [3].

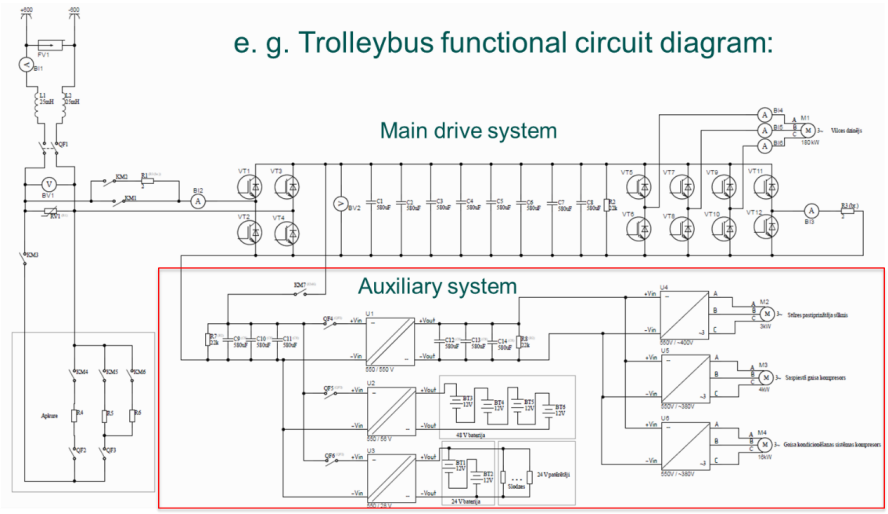


Figure 1. Example of a typical trolleybus electric power circuit functional diagram

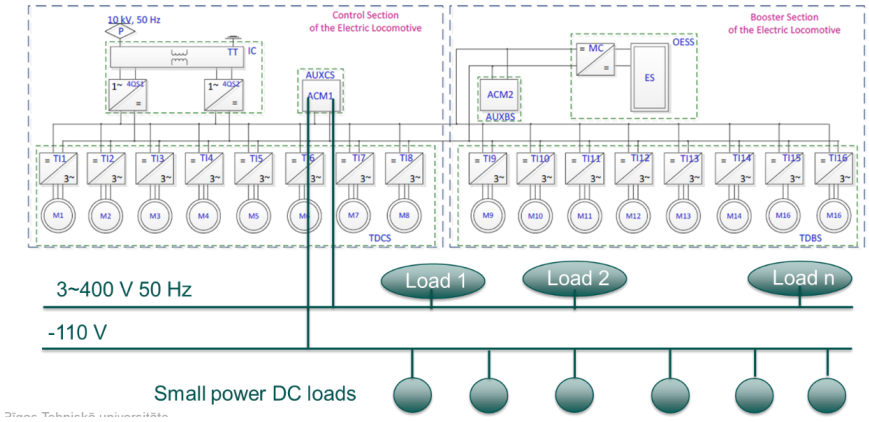


Figure 2. Example of a railway locomotive power circuit functional diagram

As can be seen from (Fig. 1.) and (Fig. 2), the diagram consists of the main drive system and the auxiliary system. The auxiliary system can be divided into 2 major parts – small loads supplied from the DC system and large loads and auxiliary drives, supplied by the AC system. The rising auxiliary system power demand trends require higher power ratings and increased efficiency in auxiliary converters, but currently the main solution is seen as increasing the converter weight and dimensions or install multiple converters in parallel. Another problem arises in the DC system supply for many relatively small loads. As there is a large number of DC loads with unpredictable mission profiles, the voltage regulation problem arises and this requires innovative solutions for the DC converter design and control to ensure a very dynamic power supply. A single DC/AC inverter is used for supplying a finite number of loads with relatively large power drawn from the AC system. In case of the simultaneous load turn on, an overcurrent or overload due to the transients might happen, moreover, in case of the converter failure the whole AC system including safety critical loads will fail. Finally, the conservative design of the auxiliary system supply leads to low efficiency, wasted energy and very dynamic load character leading to thermal cycling, shorter component lifetime and less reliable operation.

The largest part of auxiliary power is consumed by auxiliary drives, i.e., power steering, air compressor and air conditioning system. Hence, an optimization of these systems is the most reasonable. In [4], a permanent magnet synchronous machine is proposed to increase efficiency and reliability of a 6-kW auxiliary oil pump, requiring variable frequency drive supply. Similarly, in [5] the integrated variable frequency drives are recommended for both propulsion and auxiliary system drives to achieve high efficiency, reduced weight and compact design. According to case study in [6], the multi-level inverter topology realized with wide bandgap semiconductors can offer excellent performance, that is essential for variable frequency auxiliary system drives in transportation application. Consequently, the multi-level DC/AC inverter realized with SiC or GaN semiconductors can be considered as an optimal solution.

An effective solution for the non-isolated DC/DC auxiliary converter with high requirements for dynamic performance is the multiphase bidirectional buck converter with coupled inductor topology. Multi-phase DC converters are widely used in different applications, as their interleaved operation principle ensures high efficiency and low output current ripple in comparison with single phase converters [7]-[24]. Multi-phase bi-directional buck converters meet the requirements for automotive application, where different voltage levels must be interconnected with improved dynamic performance and no galvanic isolation is required between input and output [7]-[10]. The multiphase converters with coupled inductors ensure even a better solution, because they provide even higher efficiency, low phase current ripples, compact design due to reduced inductor core volume and high energy density [7]-[13] [23] [24]. However, a big issue of coupled inductor converters is a necessity of phase current balancing controller implementation, as even small differences in inductor volt-second products cause significant phase current misbalance, leading to efficiency decrease, enlarged current and voltage ripples, inductor core saturation and even converter failure [10]. Hence, the differences between all phase inductor currents must be determined and controlled to operate converter efficiently and avoid system failure.

1. SENSING AND MEASUREMENT IN AUXILIARY CONVERTERS

Sensing and measurement techniques play a crucial role in auxiliary converters. To design an intelligent and reliable control system, the main converter parameters, i.e. voltage and current must be determined or estimated. This chapter describes the general approach for cost effective and reliable current sensing techniques for multiphase converters, using single sensor, and introduces the novel Indirect Current Measurement (ICM) technique that can be used in multiphase DC/DC converters and DC/AC inverters.

1.1. General approach for current measurement using single sensor

Multi-phase DC converters are widely used in different applications, as their interleaved operation principle ensures high efficiency and low output current ripple in comparison with single phase converters. However, a significant challenge for multi-phase converters is a necessity of current balancing controller implementation, as phase current misbalance reduces efficiency, increases current and voltage ripples and even can lead to core saturation and converter failure [10]. Implementing a separate current sensor for each converter phase would be a very expensive solution [11]-[13]. In [20] a single sensor scheme is proposed, however additional switches are required to perform measurements. In [14]-[16] sensorless current sharing techniques are described, but [15] and [18] showed significant errors between the phase current values and [14] showed slow transient response. Therefore, a lot of attention recently attracted single current sensor schemes deploying the DC-link current measurement with the following phase-current reconstruction algorithms [11]-[13], [17]-[20]. It is shown in [11]-[13], that current sharing based on single DC link current sensor measurements is possible in coupled inductor converters with small errors and good transient behaviour.

As shown in [4], the DC link current can be mathematically represented by (1.1) as the sum of phase current and PWM switching function products. The PWM switching function is represented by (1.2). Considering (1.1) and (1.2), in an interleaved N-phase converter phases are shifted by T/N, therefore, the DC link current may contain the sum of 0 up to N phase currents depending on duty cycle range and, hence, N duty cycle ranges must be analysed. From measurements of the DC link current at each phase PWM carrier valley and peak points, the corresponding sum of phase currents is obtained [7]. These results are then represented by (1.3) and (1.4), respectively, where A_{vi} and A_{pi} are NxN matrices.

$$I_{DC}(t) = \sum_{i=1}^{N} I_i(t) \cdot S_i(t) \tag{1.1.}$$

where I_i – phase current, A;

S_i – PWM switching function.

$$S_i(t) = \begin{cases} 1 \; if \; 0 + \varphi_i < t < D_i \cdot T + \varphi_i \\ 0 \; if \; D_i \cdot T + \varphi_i < t < T + \varphi_i \end{cases} \tag{1.2.}$$

where φ_i – phase shift, s;

T – PWM switching period;

D_i – duty cycle.

$$\begin{bmatrix} I_{v1} \\ \vdots \\ I_{vN} \end{bmatrix} = \overline{A_v} \cdot \begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix} \tag{1.3.}$$

where I_{vi} – measurement of the DC link current at i-phase PWM carrier valley point, A;

$\overline{A_v}$ – PWM carrier valley point current reconstruction matrix.

$$\begin{bmatrix} I_{p1} \\ \vdots \\ I_{pN} \end{bmatrix} = \overline{A_p} \cdot \begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix} \tag{1.4.}$$

where I_{pi} – measurement of the DC link current at i-phase PWM carrier peak point, A;

$\overline{A_p}$ – PWM carrier peak point current reconstruction matrix.

The dependency between PWM carriers and current waveforms with DC link current sensing solution is shown on a 3-phase converter example for 3 duty cycle ranges in (Fig. 1.1.). The resultant A_{v12} 3x3 matrix with the DC link current samples at the PWM valley points valid for the duty cycle range of D∈ [0…2/3] is represented by (1.5). The resultant A_{p23} 3x3 matrix with the DC link current samples at the PWM peak points valid for the duty cycle range of D∈ [1/3…1] is represented by (1.6).

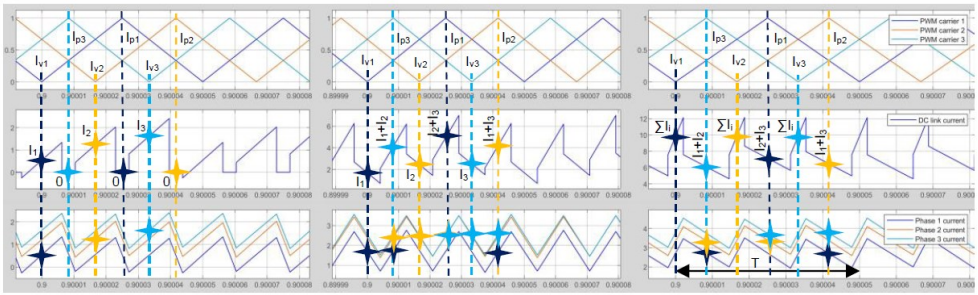


Figure 1.1. 3-phase converter current waveforms, a) D<1/3, b) 1/3<D<2/3, c) D>2/3

$$\overline{A_{v1}} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.5.}$$

$$\overline{A_{p2}} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \tag{1.6.}$$

Current reconstruction algorithms are derived for each duty cycle range by inversing the matrices A_{vi} and A_{pi} and, hence, the phase current average values are obtained from the DC link current measurements. The inversion of matrices A_{v12} and A_{p23} gives (1.7) and (1.8), valid for the duty cycle ranges D∈ [0…2/3] and D∈ [1/3…1], respectively. Consequently, there are 2 phase current reconstruction algorithms derived in the case of a 3-phase converter, valid for the duty cycle ranges D∈ [0…2/3] and D∈ [1/3…1] and represented by (1.9) and (1.10), respectively.

$$(\overline{A_{v1}})^{-1} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.7.}$$

$$\left(\overline{A_{p2}}\right)^{-1} = \frac{1}{2} \cdot \begin{bmatrix} -1 & 1 & 1 \\ 1 & -1 & 1 \\ 1 & 1 & -1 \end{bmatrix} \tag{1.8.}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \end{bmatrix} \tag{1.9.}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} -1 & 1 & 1 \\ 1 & -1 & 1 \\ 1 & 1 & -1 \end{bmatrix} \cdot \begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{p3} \end{bmatrix} \tag{1.10.}$$

The limitations of the proposed method arise when any of the matrices A_{vi} or A_{pi} becomes singular. This happens if they consist of zeros or ones, or the number of summed phase currents in the corresponding DC link current measurements has the same multiplier as the converter number of phases N. An example situation with the method limitation arises in case of a 4-phase converter operating at the duty cycle of D=0.5 point. In this case the current samples will achieve undefined values. By setting up the auxiliary current samples in between the PWM carrier valley and peak points, the obtained current sample and the phase current average value equation is (1.11). However, the 4x4 matrix A_{aux} in (1.11.) is singular and, therefore, the current reconstruction algorithm cannot be derived.

$$\begin{bmatrix} I_{t1} \\ I_{t2} \\ I_{t3} \\ I_{t4} \end{bmatrix} = \overline{A_{aux}} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{1.11.}$$

A similar situation can be observed in the case of a 6-phase converter operating in the duty cycle range D∈ [1/3…2/3]. In this case the obtained current sample and the phase current average value equation is given by (1.12) and both 6x6 matrices A_{vi} and A_{pi} are singular.

$$\begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \\ I_{v4} \\ I_{v5} \\ I_{v6} \end{bmatrix} = \begin{bmatrix} I_{p4} \\ I_{p5} \\ I_{p6} \\ I_{p1} \\ I_{p2} \\ I_{p3} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} \tag{1.12.}$$

Hence, the limitations occur only in converters with composite number of phases N within the separate duty cycle ranges. Thus, for converters with prime number of phases a general approach can specified as shown in (Fig. 1.2.).

Duty cycle range		0…1/N	1/N…2/N	2/N…3/N	…	(N-3)/N…(N-2)/N	(N-2)/N…(N-1)/N	(N-1)/N…1
Number of summed phase currents at DC link current measurement from…	valley	1	1	3	…	N-2	N-2	N
	peak	0	2	2	…	N-3	N-1	N-1
Reconstruction algorithm from measurements at…	valley	algorithm 1		alg. 3	…	algorithm N-2		-
	peak	-	algorithm 2		…	alg. N-3	algorithm N-1	

Figure 1.2. General approach for DC link current sensing and phase current reconstruction

The performed current waveform analysis shows a clear dependency between the DC link and phase current waveforms. For converters with prime number of phases, single DC link current sensor measurements can be used for phase current reconstruction within the whole duty cycle range. For converters with composite number of phases, the limitations of duty cycle ranges will occur, when using a single sensor, or a reduced number of DC link current sensors can be used to ensure operation within the whole duty cycle range. The described current measurement concept is valid for multi-phase uncoupled and coupled inductor converters with any number of phases.

1.2. Indirect current measurement in multiphase DC converter

Previously described DC link current measurements were performed directly [11]-[13] because the converter contains only one DC link capacitor with sensor position between the DC link and the half-bridges, as shown in (Fig. 1.3.a). However, if the sensor position is changed as shown in (Fig. 1.3.b), the DC link current must be obtained indirectly. The DC link current is obtained indirectly using capacitor voltage by means of (1.13).

$$I_s = I_{s1} + I_{s2} \ldots + I_{sN} = I - I_C = I - C\frac{dV_C}{dt} \tag{1.13.}$$

where I_s –DC link current, A;

I_{si} – current flowing into i-half bridge, A;

C – DC link capacitance, F;

V_C – DC link capacitor voltage, V.

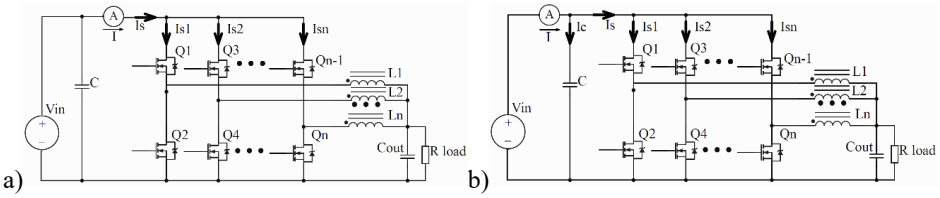


Figure 1.3. Multi-phase converter with coupled inductors and a) previously [9]-[11] used sensor position, b) proposed sensor position together with capacitor current determined by capacitor voltage measurement

In low voltage converters, where MOSFETs with low on-state resistance and breakdown voltage are used, the path length between the half-bridge switches and capacitor must be kept

minimal to avoid transient overvoltage caused by path parasitic inductance. To achieve that, an installation of capacitors, located near each of the half-bridges, would be suggested. Thus, a multi-phase converter with multiple distributed DC link capacitors is obtained as in (Fig. 1.4.). The DC link current for a 5-phase converter can be expressed by (1.14), considering the current sensor measurement and currents, flowing into the distributed DC link capacitors. Rearranging (1.14) for capacitor voltages gives (1.15).

$$I_s = I_{s1} + I_{s2} + I_{s3} + I_{s4} + I_{s5} = -I - I_{c1} - I_{c2} - I_{c3} - I_{c4} - I_{c5} \quad (1.14.)$$

where I_{ci} – current flowing into i-distributed DC link capacitor, A.

$$I_s = -I - C_1 \frac{dV_{c1}}{dt} - C_2 \frac{dV_{c2}}{dt} - C_3 \frac{dV_{c3}}{dt} - C_4 \frac{dV_{c4}}{dt} - C_5 \frac{dV_{c5}}{dt} \quad (1.15.)$$

where C_i – distributed DC link i-capacitance, F;

V_{ci} – distributed i-DC link voltage, V.

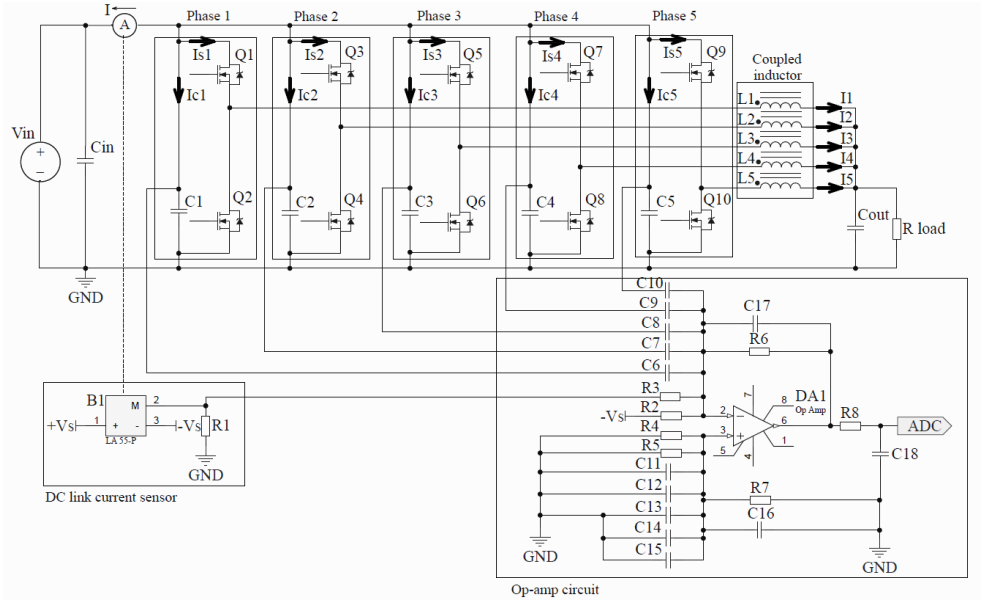


Figure 1.4. Investigated 5-phase converter with coupled inductor circuit diagram with an operational amplifier circuit for indirect current sensing

A summing differential amplifier circuit is designed, based on (1.15) considering reverse direction of the input current sensor. Additionally, an offset voltage for bidirectional current sensing and internal PT_1 performance is included by adding capacitor C_{17} in the feedback loop. Applying Kirchhoff's Current Law to the inverting input and considering the Hall effect current sensor winding ratio gives (1.16) for an op-amp circuit output signal. By neglecting the current I_{C17} from the (1.15) the scaling factor between converter currents and acquired signal are obtained by (1.17).

$$C_{17} \frac{dV_{sig}}{dt} + \frac{V_{sig}}{R_6} = \frac{V_s}{R_2} + I \cdot \frac{N_1}{N_2} \cdot \frac{R_1}{R_1 + R_3} - C_6 \frac{dV_{c1}}{dt} - C_7 \frac{dV_{c2}}{dt} - C_8 \frac{dV_{c3}}{dt} - C_9 \frac{dV_{c4}}{dt} - C_5 \frac{dV_{c5}}{dt} \quad (1.16.)$$

where V_{sig} – operational amplifier output voltage, V;

$\frac{N_1}{N_2}$ – Hall effect current sensor winding ratio;

C_i – i-capacitance, F;

R_i – i-resistance, Ω;

V_s – Hall effect current sensor supply voltage.

$$V_{sig} = V_s \cdot \frac{R_6}{R_2} + I \cdot \frac{N_1}{N_2} \cdot \frac{R_6 \cdot R_1}{R_1 + R_3} - \\ -I_{c1} \cdot \frac{R_6 \cdot C_6}{C_1} - I_{c2} \cdot \frac{R_6 \cdot C_7}{C_2} - I_{c3} \cdot \frac{R_6 \cdot C_8}{C_3} - I_{c4} \cdot \frac{R_6 \cdot C_9}{C_4} - I_{c5} \cdot \frac{R_6 \cdot C_{10}}{C_5} \quad (1.17.)$$

To increase an op-amp circuit immunity against common and differential mode disturbances, it is designed as fully symmetric differential amplifier and additionally a small output low-pass filter is applied, consisting of R8 and C18. Thus, a filtered signal is obtained, representing the restored DC link current waveforms. The obtained signal can now be used by ADC converter for DC link current measurement and phase current reconstruction, as described in the previous subchapter 1.1.

As shown in subchapter 1.1, by knowing the switching function pattern for each of the 5 duty cycle ranges, phase currents can be obtained from the DC link current samples. The switching patterns for measurements on PWM carrier valley points I_{vi} for the duty cycle ranges D<0.4 and 0.4<D<0.8 are represented by (1.18) and (1.19), respectively. The switching patterns for measurements on PWM carrier peak points I_{pi} for duty cycle ranges 0.2<D<0.6 and D<0.6 are represented by (1.20) and (1.21), respectively.

$$\begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \\ I_{v4} \\ I_{v5} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \quad (1.18.)$$

$$\begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{p3} \\ I_{p4} \\ I_{p5} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \quad (1.19.)$$

$$\begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \\ I_{v4} \\ I_{v5} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \quad (1.20.)$$

$$\begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{p3} \\ I_{p4} \\ I_{p5} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \quad (1.21.)$$

Phase currents are reconstructed from the DC link current measurements by simply inversing the 5x5 matrices for each duty cycle range. Hence, 4 current reconstruction algorithms are derived for duty cycle ranges D<0.4, 0.2<D<0.6, 0.4<D<0.8 and D<0.6, represented by (1.22), (1.23), (1.24) and (1.25), respectively.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \\ I_{v4} \\ I_{v5} \end{bmatrix} \tag{1.22.}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -1 & 1 & 1 & -1 \\ -1 & 1 & -1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & 1 & -1 \\ -1 & 1 & 1 & -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{p3} \\ I_{p4} \\ I_{p5} \end{bmatrix} \tag{1.23.}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} -1 & 2 & -1 & -1 & 2 \\ 2 & -1 & 2 & -1 & -1 \\ -1 & 2 & -1 & 2 & -1 \\ -1 & -1 & 2 & -1 & 2 \\ 2 & -1 & -1 & 2 & -1 \end{bmatrix} \cdot \begin{bmatrix} I_{v1} \\ I_{v2} \\ I_{v3} \\ I_{v4} \\ I_{v5} \end{bmatrix} \tag{1.24.}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \frac{1}{4} \cdot \begin{bmatrix} -3 & 1 & 1 & 1 & 1 \\ 1 & -3 & 1 & 1 & 1 \\ 1 & 1 & -3 & 1 & 1 \\ 1 & 1 & 1 & -3 & 1 \\ 1 & 1 & 1 & 1 & -3 \end{bmatrix} \cdot \begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{p3} \\ I_{p4} \\ I_{p5} \end{bmatrix} \tag{1.25.}$$

Simulation of a 5-phase converter with the op-amp circuit, shown in (Fig. 1.4), is performed to obtain the current waveforms, signal formed by the operational amplifier circuit and to validate the phase current reconstruction algorithms. The correspondence between simulated converter current waveforms, PWM and op-amp circuit signals in shown in (Fig. 1.5). As can be seen from (Fig. 1.5), the op-amp circuit can restore the DC link current waveforms and sampled values correspond to phase current average values. Simulations are performed for validation of the derived phase current reconstruction algorithms. An example of simulation results, when converter operates with a duty cycle D=0.3 and unbalanced phase currents are reconstructed by means of (1.23), is shown in (Fig. 1.6). As can be seen from (Fig. 1.6), phase current values can be reconstructed from indirect DC link current measurements and phase misbalance detected.

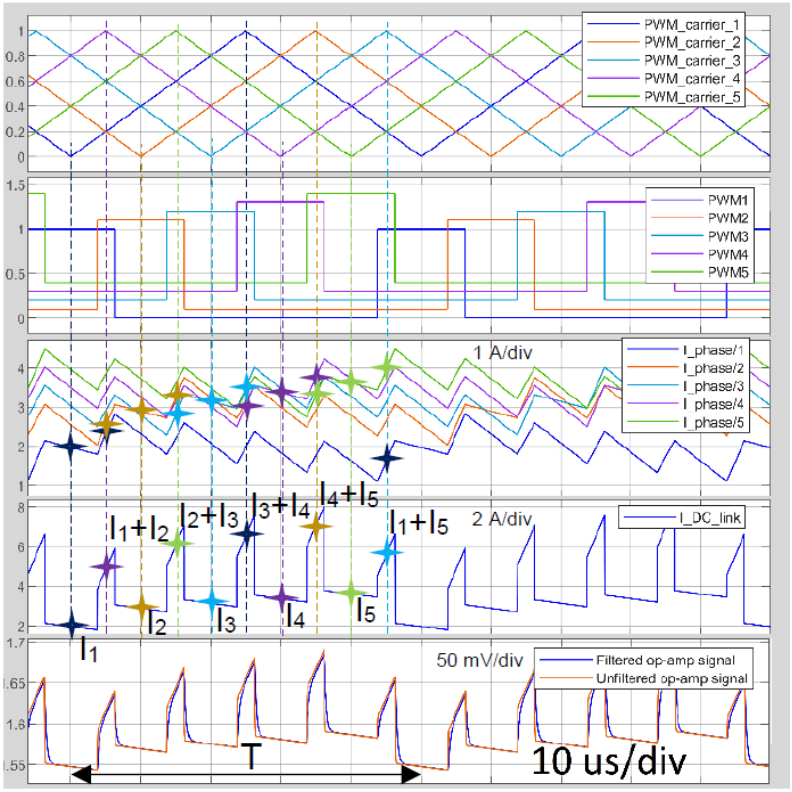


Figure 1.5. Correspondence between simulated converter current waveforms, PWM and op-amp circuit signals

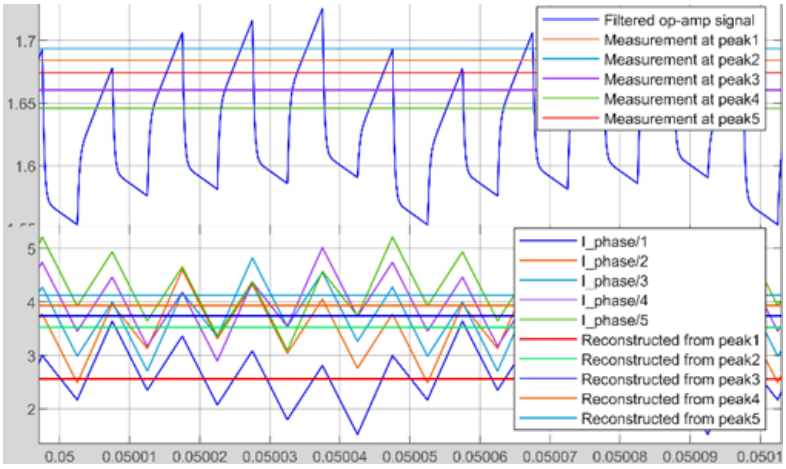


Figure 1.6. Phase current reconstruction example for 0.2<D<0.6

The proposed concept of ICM has been validated experimentally. A 5-phase buck converter with coupled inductor and distributed DC link capacitors, shown in (Fig. 1.7), is used for experimental setup. Converter circuit diagram corresponds to (Fig. 1.4), parameters are listed in (table 1.1).

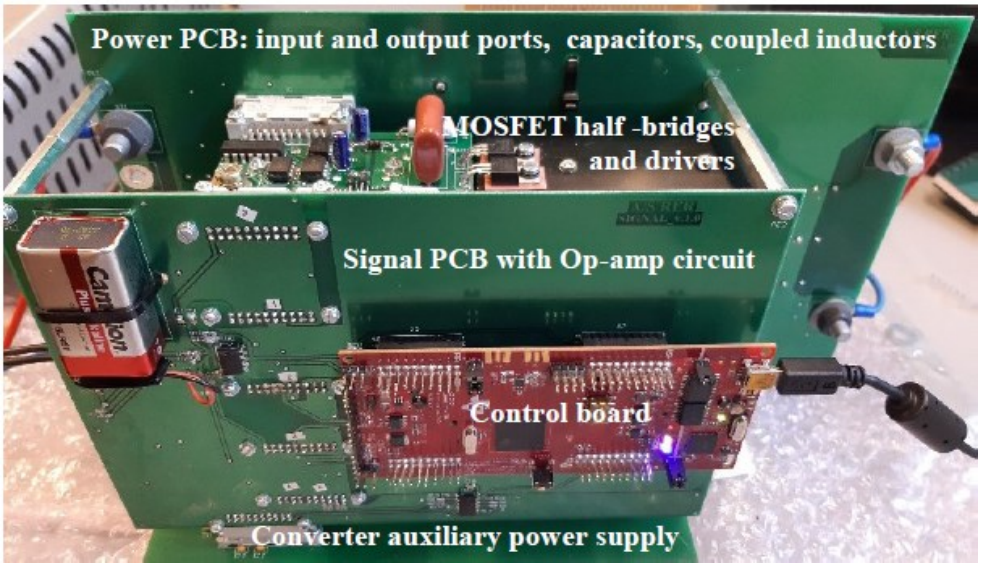


Figure 1.7. Prototype 5-phase converter with coupled inductors and ICS circuit

Table 1.1.

Prototype converter circuit parameters

Parameter, designator	Values
Input voltage Vin	24-60 V
Load Rload	0.1-10 Ω (500 W)
Switching frequency f	50 kHz
Cin	100 nF
Cout	3 mF
C1…C5	10 µF
Sensor type and winding ratio N1:N2	LA 55-P, 1:1000
MOSFET Q1…Q10	IRF135B203
Op-amp DA1	AD845JNZ
R1, R8	95.3 Ω
R2, R4	10 kΩ
R3, R5	857.7 Ω
R6, R7	1 kΩ
C6…C15	1 nF
C16, C17	120 pF
C18	470 pF

Firstly, the indirectly acquired DC link current waveforms are compared with the phase current waveforms under normal operating conditions. The cases with balanced and unbalanced phase currents are shown in (Fig. 1.8.) a and b, respectively. In the first case, phase currents are

almost equal and therefore, the restored DC link current waveform is lined-up with sampled values nearly same. In case of misbalance, the phase currents are inequal and the signal obtained from op-amp circuit reflects an existing phase current misbalance. Secondly, the current measurement accuracy is investigated. The differences between reconstructed and measured phase current values are compared at different converter operating points within the whole duty cycle range. The resulted deviations are shown in (Fig. 1.9.). The accuracy of the proposed method is adequate, phase current misbalance is well represented by the ICM sensing signal and the measurement error is well below 0.5 A in the wide operation range.

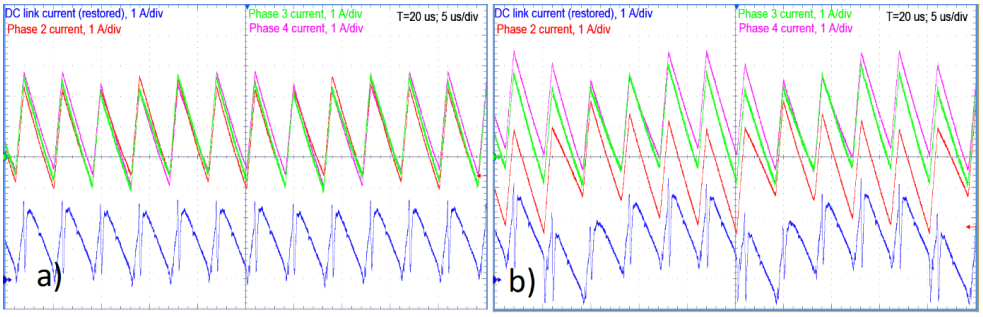


Figure 1.8. Converter current waveforms under normal operating conditions in case of a)balanced and b)unbalanced phase currents

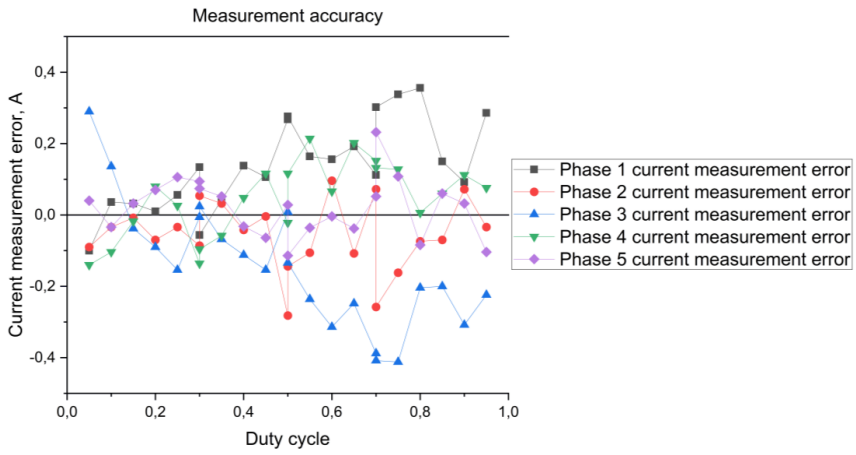


Figure 1.9. Deviations between measured and reconstructed phase current values

The DC link current waveforms can be restored in good quality using a single current sensor with an operational amplifier circuit in converters with distributed DC link capacitors. 4 phase current reconstruction algorithms are derived for the 5-phase converter operation within the whole duty cycle range. Simulation and experimental results approve the proposed technique. The precision of acquired current measurements achieved measurement errors below 0.5 A and is influenced by signal filtering, differences between phase-to-phase impedances and passive

component tolerances. Achieved accuracy in real operating conditions, nevertheless, is adequate for a current balancing controller implementation, as approved in [25].

1.3. Indirect current measurement in multi-level inverter

The dependency between the DC link and phase currents in inverters have been investigated in [26]-[35]. The cost reduction in current sensing infrastructure of a 2-level inverter is achieved by implementing a single DC-link current sensor at converter input. Using single sensor for performing multiple measurements distributed within the switching period and following implementing of the phase current reconstruction algorithms has shown significant overall system price reduction and possibility of additional fault-tolerant technique implementation, in case phase current sensors are used anyway [33], [34]. Phase current reconstruction in 3-level inverter, using single neutral DC link current sensing shunt is described in [26], [28]-[31]. This technique is the most advantageous, however [27] showed, that some limitations still apply, when only single sensor is used.

PWM inverter current sensing solution must ensure not only the current value detection, but also protection against isolation faults and short circuits [33]. Shin and Ha [27] showed, that the phase currents can be reconstructed using single (SDSS) or multiple (MDSS) top (TSS), bottom (BSS) and neutral (NSS) DC link shunt sensing. Nonetheless, a combination of at least 2 (multiple) DC link current shunts are required to ensure full inverter protection and minimize current unmeasurable areas (CUA) by reconstructing phase currents using space vector pulse width modulation (SVPWM) [27]. In terms of costs, this is comparable with use of phase current sensors. Shin and Ha emphasize, that shunt current sensing was originally designed for protection purposes, but additionally “the MDSS technique becomes a cost-effective current measurement method” [27]. Hence, this technique is economically effective, but challenging from the design perspective.

The direct DC link current sensor placement is rather difficult if not impossible to implement in a common inverter design with planar bus bars. Lu et al. [35] faces this problem in 2-level inverters and proposes an input current measurement to ensure fault tolerant operation by current estimation in case of phase current sensor fault. Thus, the path length between the inverter phase legs and DC link capacitors can be kept minimal, and the parasitic inductance caused effects can be minimized [35]. This allows using lower voltage rated semiconductor devices, i.e., SiC MOSFETs, with significantly higher switching frequencies in typical inverter applications.

Hence, the indirect measurement approach can be extended for a multi-level inverter with planar busbars between DC link capacitors and switching devices, by placing an input current sensor at the positive DC rail. Additionally, 2 operational amplifier circuits are implemented to restore the top (TDC) and neutral (NDC) DC link current waveforms, thus, ensuring indirect fault tolerant multiple DC link current sensing (MDCS) [26]-[29] by means of single sensor and sensorless sensing techniques, respectively. The indirect multiple DC link current sensing (MDCS) technique is analysed on a 3-phase 3-level neutral point diode clamped PWM inverter example, which is shown in (Fig.1.10) with the corresponding operational amplifier circuits

used for DC link current waveform restoration. Using (Fig. 1.10), the top and neutral DC link currents and can be expressed by means (1.26) and (1.27).

$$I_{TDC} = -I_{in} - I_{C1} = -I_{in} - C_1 \frac{dV_{c1}}{dt} \tag{1.26.}$$

where I_{c1} – current flowing into top DC link capacitor, A;

I_{in} – input current at the positive rail, A;

C_1 – top DC link capacitance, F;

V_{c1} – top DC link voltage, V.

$$I_{NDC} = I_{C1} - I_{C2} = C_1 \frac{dV_{c1}}{dt} - C_2 \frac{dV_{c2}}{dt} \tag{1.27.}$$

where I_{c2} – current flowing into bottom DC link capacitor, A;

C_2 – bottom DC link capacitance, F;

V_{c2} – bottom DC link voltage, V.

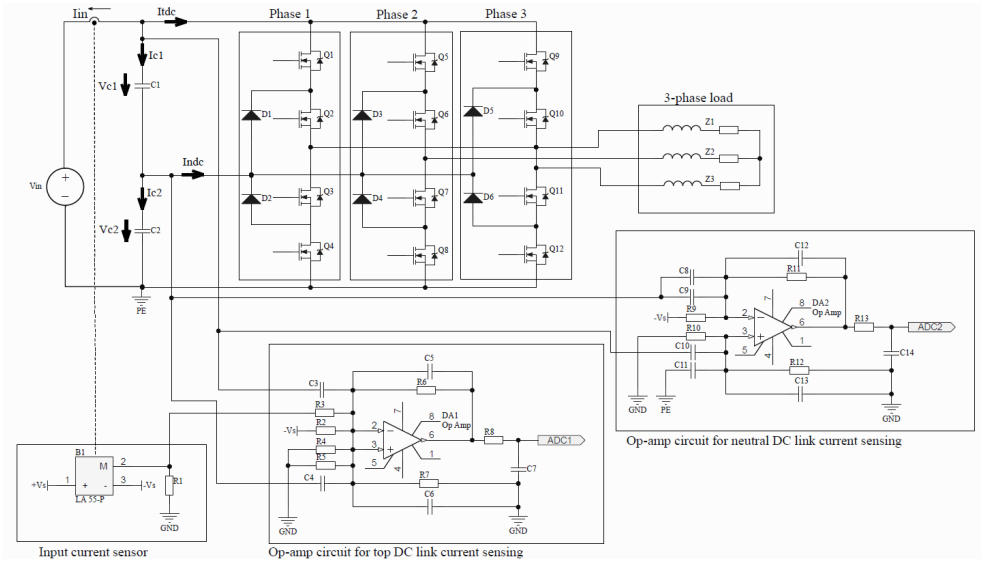


Figure 1.10. Investigated 3-phase 3-level neutral point diode clamped inverter circuit diagram with 2 operational amplifier circuits for indirect current sensing

Both operational amplifier circuits are fully symmetric and filter parameters are chosen to ensure high frequency component (e.g. voltage ringing) and common mode noise elimination, but the low frequency components remain almost unaffected in terms of amplitude and phase shift. An op-amp DA1 circuit is designed to restore the TDC waveforms. Applying Kirchhoff's Current Law to the inverting input and considering reverse direction with winding ratio of the sensor N_1/N_2 gives (1.28) for an op-amp DA1 circuit output signal V_{ADC1}. By neglecting the current I_{C5} scaling factor between inverter TDC and acquired signal are obtained by (1.29). An op-amp DA2 is designed to restore the NDC waveforms. Applying Kirchhoff's Current Law to the inverting input gives (1.30) for an op-amp DA2 circuit output signal V_{ADC2}. By neglecting the current I_{C12} scaling factor between inverter NDC and acquired signal are obtained by (1.31).

$$C_5 \frac{dV_{ADC1}}{dt} + \frac{V_{ADC1}}{R_6} = \frac{V_s}{R_2} + I_{in} \cdot \frac{N_1}{N_2} \cdot \frac{R_1}{R_1+R_3} - C_3 \frac{dV_{c1}}{dt} \quad (1.28.)$$

where V_{ADC1} – operational amplifier output voltage for TDC, V;

$\frac{N_1}{N_2}$ – Hall effect current sensor winding ratio;

C_i – i-capacitance, F;

R_i – i-resistance, Ω;

V_s – Hall effect current sensor supply voltage.

$$V_{ADC1} = V_s \cdot \frac{R_6}{R_2} + I_{in} \cdot \frac{N_1}{N_2} \cdot \frac{R_6 \cdot R_1}{R_1+R_3} - I_{c1} \cdot \frac{R_6 \cdot C_3}{C_1} \quad (1.29.)$$

$$C_{12} \frac{dV_{ADC2}}{dt} + \frac{V_{ADC2}}{R_{11}} = \frac{V_s}{R_9} + C_{10} \frac{dV_{c1}}{dt} - C_9 \frac{dV_{c2}}{dt} \quad (1.30.)$$

where V_{ADC2} – operational amplifier output voltage for TDC, V;

C_i – i-capacitance, F;

R_i – i-resistance, Ω.

$$V_{ADC2} = V_s \cdot \frac{R_6}{R_2} + I_{in} \cdot \frac{N_1}{N_2} \cdot \frac{R_6 \cdot R_1}{R_1+R_3} - I_{c1} \cdot \frac{R_6 \cdot C_3}{C_1} \quad (1.31.)$$

Current measurements can be performed by setting up the sampling points within the possible measurement windows. To acquire multiple current measurements within a period, the switching states in a single measurement window must be constant. Moreover, the current unmeasurable areas, containing switching transients and voltage ringing effects, must be avoided. The minimal PWM state length, suitable for DC link current measurement is depicted by means of (Fig. 1.11). It should last for at least the time interval T_{min}, consisting of driver delay with the time of switching transient T_{delay}, and include current sample acquisition delay $T_{S\&H}$. If the actual PWM state length is shorter, than the time interval T_{min}, the corresponding measurement is not performed. Nonetheless, it is assured, that the number of samples within one sine period will be enough, if at least 10 switching periods are within one sine period. However, the Nyquist criteria can be fulfilled, if at least 2 valid measurements are performed within a sine period and with MDCS this can be achieved by at least one TDC and one NDC samples.

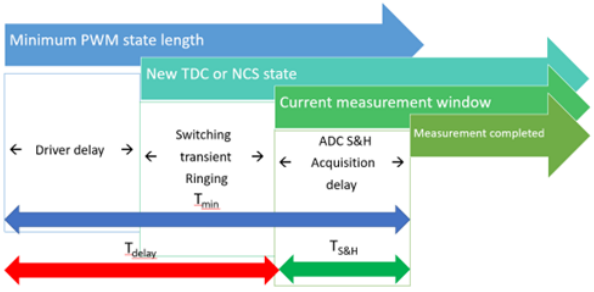


Figure 1.11. Minimal PWM state length requirement for current measurement window

Phase currents are reconstructed from the corresponding DC link current measurements by knowing the actual switching states [27]. The correspondence between switching states, additional requirements for reliable current measurement, as well as the TDC and NDC value correspondence to the phase current values is shown in (table 1.2). The phase current sum is assumed to be equal to zero and, therefore, phase current values can be represented by (1.32). Here, the corresponding phase duty cycle (D_i) values are assumed to be positive ($D_i>0$), when the high side is switching (and the low side switch is closed), and negative ($D_i<0$), when the low side is switching (and the high side switch is open). The additional requirements are defined for triangular PWM carrier and the current measurements are set-up on the incrementing high-side switch carrier with positive duty cycle. This information is used by the current reconstruction algorithm, implemented in the microcontroller. Reconstructed phase current values can then be used for inverter controller or fault tolerant algorithm implementation.

Table 1.2.

Correspondence between switching states, requirements, TDC, NDC and phase currents

Switch states $S_1S_2S_3$	Requirements for current measurement (conditional statements)	Sampling point setup	Reconstructed phase currents	
			From TDC	From NDC
211	$TD_1 > T_{min}$ & $D_2 < 0$ & $D_3 < 0$ & $(TD_2 + T) > T_{min}$ & $(TD_3 + T) > T_{min}$	T_{delay}	I_1	$-I_1$
121	$TD_2 > T_{min}$ & $D_1 < 0$ & $D_3 < 0$ & $(TD_1 + T) > T_{min}$ & $(TD_3 + T) > T_{min}$	T_{delay}	I_2	$-I_2$
112	$TD_3 > T_{min}$ & $D_1 < 0$ & $D_2 < 0$ & $(TD_1 + T) > T_{min}$ & $(TD_2 + T) > T_{min}$	T_{delay}	I_3	$-I_3$
122	$TD_2 > T_{min}$ & $TD_3 > T_{min}$ & $D_1 < 0$ & $(TD_1 + T) > T_{min}$	T_{delay}	$-I_1$	I_1
212	$TD_1 > T_{min}$ & $TD_3 > T_{min}$ & $D_2 < 0$ & $(TD_2 + T) > T_{min}$	T_{delay}	$-I_2$	I_2
221	$TD_1 > T_{min}$ & $TD_2 > T_{min}$ & $D_3 < 0$ & $(TD_3 + T) > T_{min}$	T_{delay}	$-I_3$	I_3
210	$T(D_1 - D_2) > T_{min}$ & $D_2 > 0$ & $(TD_1 - TD_3 - T) > T_{min}$	$TD_1 - T_{S\&H}$	I_1	I_2
210	$T(D_2 - D_3) > T_{min}$ & $D_2 < 0$ & $(TD_1 - TD_2 - T) > T_{min}$	$TD_2 + T - T_{S\&H}$	I_1	I_2
201	$T(D_1 - D_3) > T_{min}$ & $D_3 > 0$ & $(TD_1 - TD_2 - T) > T_{min}$	$TD_1 - T_{S\&H}$	I_1	I_3
201	$T(D_3 - D_2) > T_{min}$ & $D_3 < 0$ & $(TD_1 - TD_3 - T) > T_{min}$	$TD_3 + T - T_{S\&H}$	I_1	I_3
120	$T(D_2 - D_1) > T_{min}$ & $D_1 > 0$ & $(TD_2 - TD_3 - T) > T_{min}$	$TD_2 - T_{S\&H}$	I_2	I_1
120	$T(D_1 - D_3) > T_{min}$ & $D_1 < 0$ & $(TD_2 - TD_1 - T) > T_{min}$	$TD_1 + T - T_{S\&H}$	I_2	I_1
021	$T(D_2 - D_3) > T_{min}$ & $D_3 > 0$ & $(TD_2 - TD_1 - T) > T_{min}$	$TD_2 - T_{S\&H}$	I_2	I_3
021	$T(D_3 - D_1) > T_{min}$ & $D_3 < 0$ & $(TD_2 - TD_3 - T) > T_{min}$	$TD_3 + T - T_{S\&H}$	I_2	I_3
102	$T(D_3 - D_1) > T_{min}$ & $D_1 > 0$ & $(TD_3 - TD_2 - T) > T_{min}$	$TD_3 - T_{S\&H}$	I_3	I_1
102	$T(D_1 - D_2) > T_{min}$ & $D_1 < 0$ & $(TD_3 - TD_1 - T) > T_{min}$	$TD_1 + T - T_{S\&H}$	I_3	I_1
012	$T(D_3 - D_2) > T_{min}$ & $D_2 > 0$ & $(TD_3 - TD_1 - T) > T_{min}$	$TD_3 - T_{S\&H}$	I_3	I_2
012	$T(D_2 - D_1) > T_{min}$ & $D_2 < 0$ & $(TD_3 - TD_2 - T) > T_{min}$	$TD_2 + T - T_{S\&H}$	I_3	I_2

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 & -1 & -1 \\ -1 & 0 & -1 \\ -1 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{1.32.}$$

where I_i – i-th phase current, A.

A simulation of a 3-phase 3-level neutral point diode clamped inverter with both op-amp circuits, shown in (Fig.1.10), is performed to obtain the SVPWM, current waveforms and the signals formed by the operational amplifier circuits. The resulting waveforms are shown in

(Fig.1.12) for current frequency of 100 Hz, modulation frequency 1 kHz and inductive load with full impedance Z=13,1 Ω and φ=17,4°(lagging). A clear dependency between top (TDC) and neutral (NDC) DC link currents on phase currents with their corresponding SVPWM states is observed. Both TDC and NDC waveforms are fully restored by their operational amplifier circuits without any visible errors or phase delays and, hence, phase currents can be reconstructed using op-amp circuit formed signals with adequate accuracy. All phase currents can be reconstructed from TDC, using at least 8, and from NDC, using at least 10 sampling points per period within large enough measurement windows. Hence, the Nyquist criteria holds even, if the sine period is equal to 10 switching periods, but inverter operation with higher switching frequency (or lower sine frequency) would allow to make even more phase current measurements per sine period, thus, reducing the current unmeasurable areas and their influence on phase current estimation capabilities.

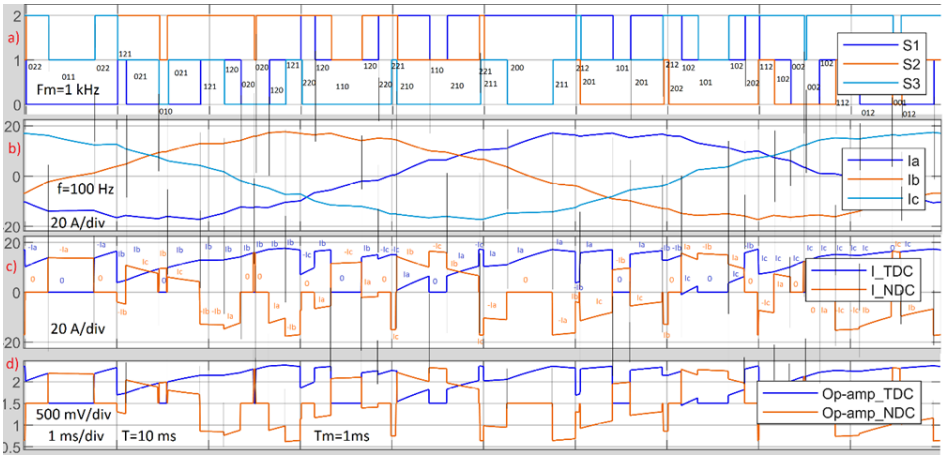


Figure 1.12. Simulation results with a) SVPWM states, b) phase currents, c) top and neutral DC link currents, d) restored TDC and NDC waveforms from op-amp circuits

The proposed concept of ICM has been validated experimentally. A prototype 3-phase 3-level neutral point diode clamped inverter with integrated TDC and NDC sensing circuits has been built for experimental verification of the proposed concept. Prototype inverter layout is shown in (Fig.1.13). Prototype circuit parameters are listed in (table 1.3).

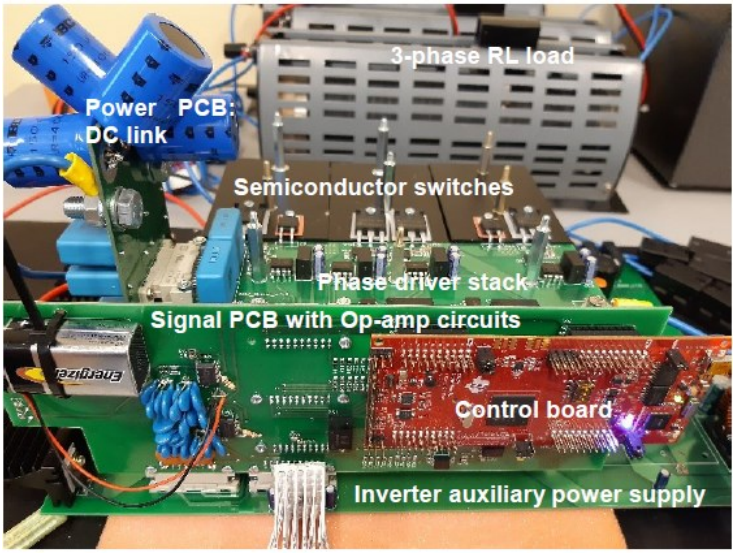


Figure 1.13. Prototype 3-phase 3-level NPC inverter layout

Table 1.3.

Prototype inverter circuit parameters

Parameters	Values for experimental prototype
DC Input voltage Vin	48-600 V
AC Output voltage (RMS) Vout	30-400 V
Load Z1, Z2, Z3	RL - adjustable
Switching frequency f	1-10 kHz
Auxiliary supply Vs	15 V
Sensor type and winding ratio N1:N2	LA 55-P, 1:1000
MOSFET Q1…Q12	IMW65R107M1HXKSA1
Diode D1…D6	IDH20G65C6XKSA1
Op-amp DA1, DA2	AD845JNZ
C1, C2	300 µF
C3, C4, C8…C11	7,5 nF
C5…C7, C12…C14	1 nF
R1, R8, R13	100 Ω
R2, R4, R9, R10	20 kΩ
R3, R5	3.9 kΩ
R6, R7, R11, R12	2 kΩ

Firstly, the correspondence of current waveforms between experimental and simulation results for switching frequency of 2 kHz is shown in (Fig. 1.14.). The calculated TDC and NDC waveforms are preserved by the op-amp circuits. Separately reconstructed phase current values are shown in (Fig. 1.15). An example phase current reconstruction outcome for the 5 kHz switching frequency is shown in (Fig. 1.16).

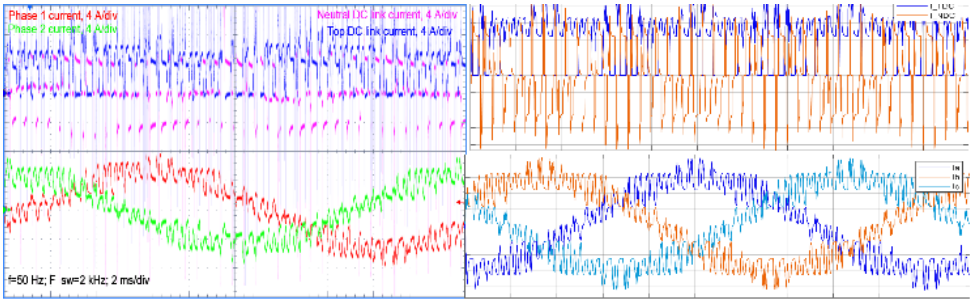


Figure 1.14. a) Experimental and b) simulated inverter current waveforms at 2 kHz switching frequency

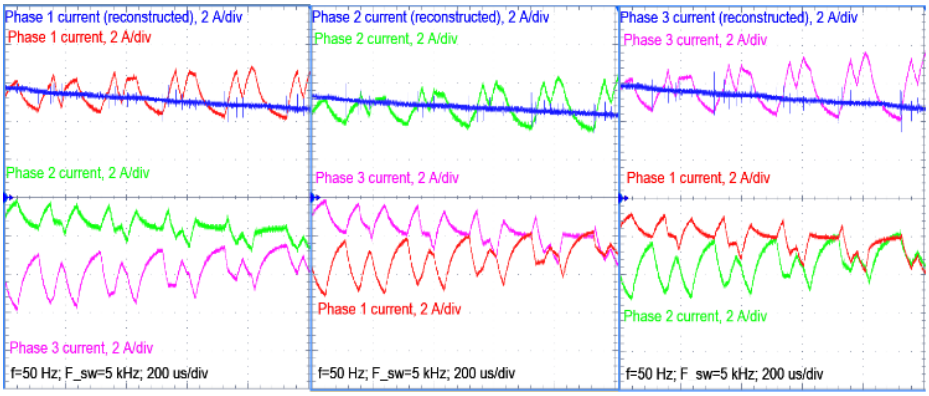


Figure 1.15. Separately reconstructed phase currents

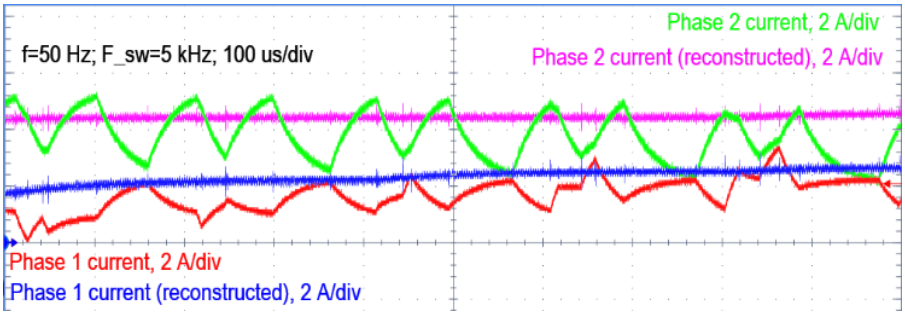


Figure 1.16. Phase current reconstruction at 5 kHz switching frequency

The indirect MDCS has shown good current waveform quality, high precision and immunity against disturbances. Further analysis of TDC and NDC current samples, by evaluating the difference between reconstructed and real phase current values has shown, that indirect DC link current sensing technique achieves an adequate measurement accuracy. The precision of acquired current measurements is mainly influenced by signal filtering, differences

between phase-to-phase impedances, passive component tolerances, DC link capacitor ESR and correct measurement window setup. With inverter switching frequencies up to 20 kHz, the reconstructed phase current value maximum measured deviation at separate points did not exceed 20 %. At most of acquired measurement points (>90%), the relative error was below 10 %. Achieved accuracy was lower at high switching frequencies and gradually improved with the frequency decrease. Hence, the indirect MDCS can be used in modern power supply and electrical drive applications. Moreover, it can be extended for multi-phase and multi-level inverters. The ICM implementation in a 3-phase 3-level inverter is specified in more details in [36].

1.4. Conclusions

The dependency between the DC link and phase current waveforms can be used for a cost effective single sensor measurements. For converters with prime number of phases, single DC link current sensor measurements can be used for phase current reconstruction within the whole duty cycle range. For converters with composite number of phases, the limitations of duty cycle ranges will occur, when using a single sensor, or a reduced number of DC link current sensors can be used to ensure operation within the whole duty cycle range.

Using an indirect DC link current measurement technique for a multi-phase DC converter with coupled inductors the DC link current waveforms can be restored in good quality using a single current sensor with an operational amplifier circuit in converters with distributed DC link capacitors. The accuracy of the proposed ICM method in multiphase DC/DC converters is adequate, phase current misbalance is well represented by the ICM sensing signal and the measurement error is well below 0.5 A in the wide operation range. Achieved precision in real operating conditions is sufficient for a current balancing controller implementation without any visible waveform or efficiency degradation.

The proposed ICM technique is valid for single sensor or sensorless phase current detection in the multi-level inverters, using TDC or NDC sensing separately. The TDC and NDC waveforms can be restored using a single current sensor with 2 operational amplifier circuits, both forming a reliable MDCS technique, used for phase current reconstruction. The indirect MDCS has been verified using simulation and experimental results and has shown good current waveform quality, high precision and immunity against disturbances. Hence, the indirect MDCS can be used in modern auxiliary power supply and drive applications.

2. AUXILIARY CONVERTER CONTROL

Auxiliary converter controller design is an essential step to achieve the objective of energetically and economically effective technology. To develop an intelligent and reliable control system with fast response, the system internal parameters and behaviour must be analysed narrowly. This chapter describes the converter system transfer function determination and controller design and analyses the fuzzy logic controller performance under different circumstances. The detailed fuzzy logic controller design is described in [37].

2.1. Coupled inductor analysis

The 5-phase DC/DC converter, considered in subchapter 1.2 is built with a coupled inductor. Coupled inductor is formed by the differential configuration of 5 toroidal N87 cores EPCOS B64290L0082X087 with 5 turns for each phase winding. The coupled inductor configuration with superimposed magnetic circuit is shown in (Fig. 2.1). The corresponding magnetic circuit diagram is shown in (Fig. 2.2.). The inductance matrix measurement results in the linear range are represented in (2.1).

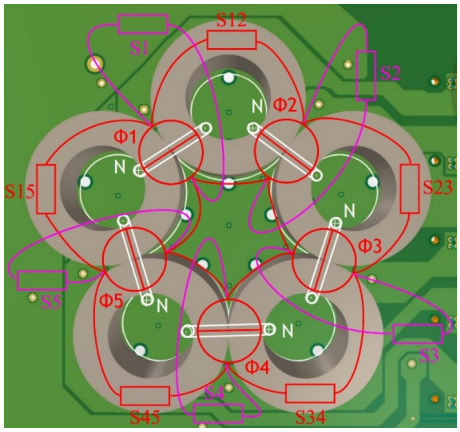


Figure 2.1. Coupled inductor configuration in converter

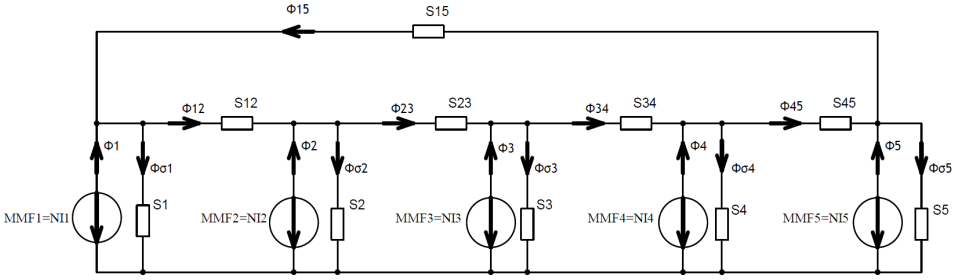


Figure 2.2. Coupled inductor magnetic circuit

$$L = \begin{bmatrix} 211 & -104 & 0 & 0 & -106 \\ -104 & 210 & -104 & 0 & 0 \\ 0 & -104 & 209 & -104 & 0 \\ 0 & 0 & -104 & 210 & -104 \\ -106 & 0 & 0 & -104 & 212 \end{bmatrix} \quad (2.1)$$

where L – inductance matrix (in linear range), μH;

The considered coupled inductor magnetic circuit diagram is analysed to obtain the mathematical model for the further non-linear analysis and determination of transfer function. By applying the superposition theorem to the magnetic circuit shown in (Fig. 2.2), an equation system (2.2) is obtained:

$$\begin{cases} \Phi_1 = \Phi_{\sigma 1} + \Phi_{12} - \Phi_{51} = \frac{MMF_1}{S_1} + \frac{MMF_1}{S_{12}} - \frac{MMF_2}{S_{12}} - \frac{MMF_5}{S_{51}} + \frac{MMF_1}{S_{51}} \\ \Phi_2 = \Phi_{\sigma 2} + \Phi_{23} - \Phi_{12} = \frac{MMF_2}{S_2} + \frac{MMF_2}{S_{23}} - \frac{MMF_3}{S_{23}} - \frac{MMF_1}{S_{12}} + \frac{MMF_2}{S_{12}} \\ \Phi_3 = \Phi_{\sigma 3} + \Phi_{34} - \Phi_{23} = \frac{MMF_3}{S_3} + \frac{MMF_3}{S_{34}} - \frac{MMF_4}{S_{34}} - \frac{MMF_2}{S_{23}} + \frac{MMF_3}{S_{23}} \\ \Phi_4 = \Phi_{\sigma 4} + \Phi_{45} - \Phi_{34} = \frac{MMF_4}{S_4} + \frac{MMF_4}{S_{45}} - \frac{MMF_5}{S_{45}} - \frac{MMF_3}{S_{34}} + \frac{MMF_4}{S_{34}} \\ \Phi_5 = \Phi_{\sigma 5} + \Phi_{51} - \Phi_{45} = \frac{MMF_5}{S_5} + \frac{MMF_5}{S_{51}} - \frac{MMF_1}{S_{51}} - \frac{MMF_4}{S_{45}} + \frac{MMF_5}{S_{45}} \end{cases} \quad (2.2)$$

where $\Phi_{\sigma i}$ – magnetic flux in the air across i-phase windings, Wb;

Φ_{ij} – magnetic flux in the torus between i- and j-phase windings, Wb;

Φ_i – magnetic flux corresponding to i-phase windings, Wb;

MMF_i – magnetomotive force across i-phase windings, A (Ampere-turns);

S_i – reluctance of the air path across i-phase windings, H^{-1};

S_{ij} – reluctance of the toroid between i- and j-phase windings, H^{-1}.

Rearranging (2.2) to the state space representation gives (2.3) that can be further used in a simulation model.

$$\begin{bmatrix} \Phi_1 \\ \Phi_2 \\ \Phi_3 \\ \Phi_4 \\ \Phi_5 \end{bmatrix} = \begin{bmatrix} (\frac{1}{S_1} + \frac{1}{S_{51}} + \frac{1}{S_{12}}) & -\frac{1}{S_{12}} & 0 & 0 & -\frac{1}{S_{51}} \\ -\frac{1}{S_{12}} & (\frac{1}{S_2} + \frac{1}{S_{12}} + \frac{1}{S_{23}}) & -\frac{1}{S_{23}} & 0 & 0 \\ 0 & -\frac{1}{S_{23}} & (\frac{1}{S_3} + \frac{1}{S_{23}} + \frac{1}{S_{34}}) & -\frac{1}{S_{34}} & 0 \\ 0 & 0 & -\frac{1}{S_{34}} & (\frac{1}{S_4} + \frac{1}{S_{34}} + \frac{1}{S_{45}}) & -\frac{1}{S_{45}} \\ -\frac{1}{S_{51}} & 0 & 0 & -\frac{1}{S_{45}} & (\frac{1}{S_5} + \frac{1}{S_{45}} + \frac{1}{S_{51}}) \end{bmatrix} \cdot \begin{bmatrix} MMF_1 \\ MMF_2 \\ MMF_3 \\ MMF_4 \\ MMF_5 \end{bmatrix} \quad (2.3)$$

where Φ_i – magnetic flux corresponding to i-phase windings, Wb;

MMF_i – magnetomotive force across i-phase windings, A (amperturns);

S_i – reluctance of the air path across i-phase windings, H^{-1};

S_{ij} – reluctance of the toroid between i- and j-phase windings, H^{-1}.

For the further non-linear analysis of the coupled inductor behaviour in converter under different ultimate operation conditions, a B-H (magnetization) curve of N87 ferrite has been is

combined with the toroid dimensions. The different mathematical models have been derived to express the non-linear dependence between the magnetic flux density B and the magnetic field strength H and shown in (Fig.2.3) by means of the B-H curve.

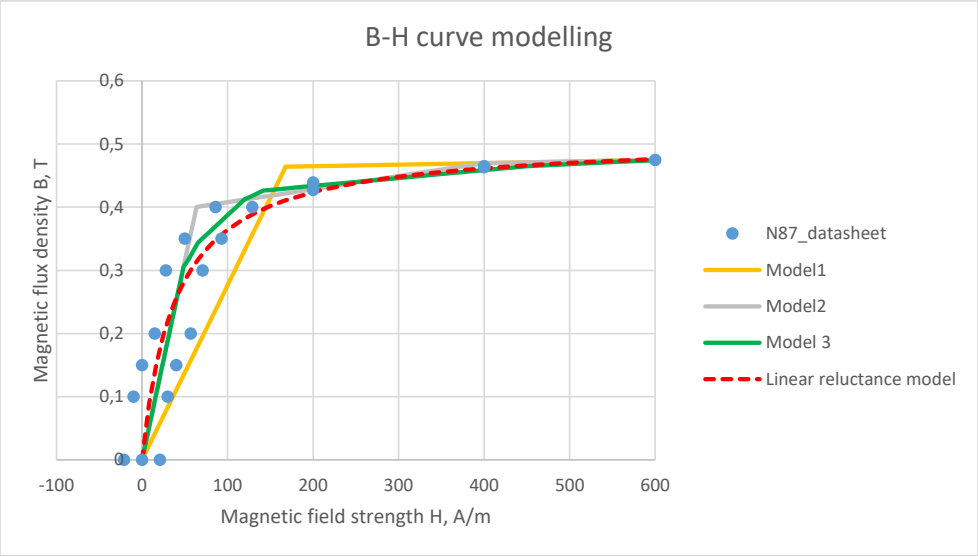


Figure 2.3. Comparison between different mathematical models, representing the non-linearity of B-H curve

The model 1 has the easiest mathematical expression and considers 2 ranges of the B-H curve, - the linear range and the saturation range. This model is the most suitable in terms of computational power requirements, however it is not accurate enough to model and analyse the partial saturation effects in the coupled inductor converter. The model 2 has a reasonable mathematical expression and considers 3 ranges of the B-H curve, - the linear range, the partial saturation range, and the full saturation range. It models the natural B-H curve well and is balanced in terms of computational power requirements, however some impreciseness of transition between the linear and partial saturation ranges might cause inappropriate analysis results. The model 3 has a more complex mathematical expression and considers 6 ranges of the B-H curve with the 6 adjusted magnetic material permittivity values, - from the linear range to the full saturation range. It follows the natural B-H curve in an excellent way, but its implementation would demand high computational power requirements, resulting in slow simulation process, therefore, is not feasible from the practical application perspective.

The linear reluctance model considers the linear dependence between the reluctance and the magnetic field strength H. In terms of the given inductor toroid dimensions, the correspondence between the magnetic flux Φ and the magnetic flux density B is expressed in (2.4), but the correspondence between the magnetomotive force MMF and the magnetic field strength H is expressed in (2.5). Hence, the reluctance S in given by linear function (2.6) shown in (Fig.2.4), dependant on the magnetomotive force. The magnetic flux Φ is then calculated from (2.7),

given the reluctance S and the magnetomotive force MMF from (2.8). The comparison between the different mathematical models is shown on the graph illustrating the coupled inductor correspondence between the magnetic flux and magnetomotive force (dependent on the phase current) in (Fig.2.5).

$$B = \frac{\Phi}{A} = \frac{\Phi}{0{,}1957 \cdot 10^{-6}} \tag{2.4.}$$

where Φ – magnetic flux in the toroid, Wb;

A – toroid core cross-sectional area, m^2;

B – magnetic flux density, T.

$$H = \frac{\text{MMF}}{l} = \frac{MMF}{0{,}12} \tag{2.5.}$$

where H – magnetic field strength, A/m;

l – toroid magnetic path length (by the centreline), m;

MMF – magnetomotive force, A (Ampere-turns).

$$S = a \cdot MMF + b = 10082 \cdot MMF + 47396 \tag{2.6.}$$

where S – reluctance, A/Wb;

a – gradient coefficient (acquired from tendency line in (Fig.2.4)), 1/Wb;

b – intercept coefficient (acquired from tendency line in (Fig.2.4)), A/Wb.

$$\Phi = \frac{MMF}{S} \tag{2.7.}$$

$$MMF = N \cdot I \tag{2.8.}$$

where N – number of turns in the phase winding;

I – current flowing in the phase windings, A.

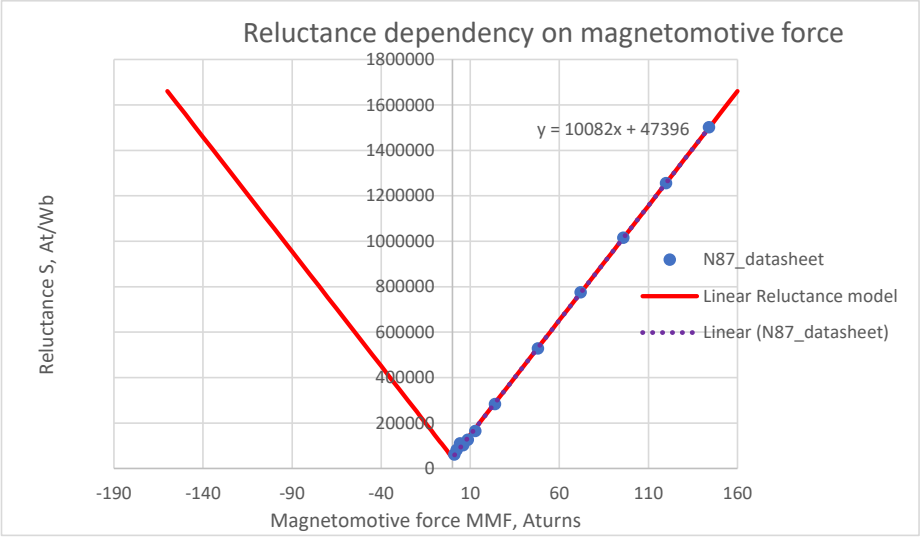


Figure 2.4. Linear reluctance model depending on the magnetomotive force

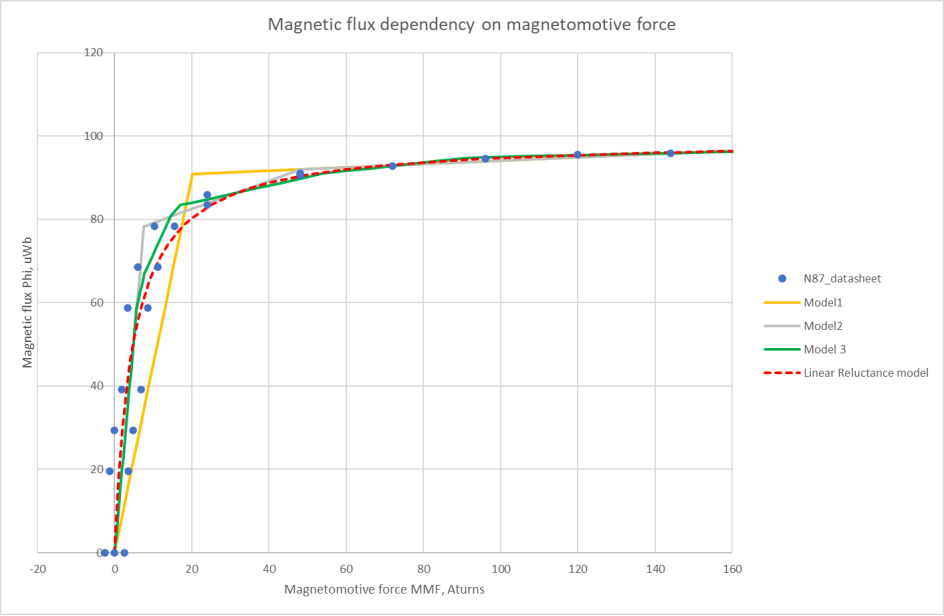


Figure 2.5. Comparison between different mathematical models superimposed on the graph illustrating the correspondence between magnetic flux and magnetomotive force

As the linear dependency model expressing the correspondence between the reluctance and the magnetomotive force follows the natural B-H curve in an accurate manner, the resultant magnetic flux dependency on magnetomotive force has been considered for the further analysis and depicted in (Fig. 2.6).

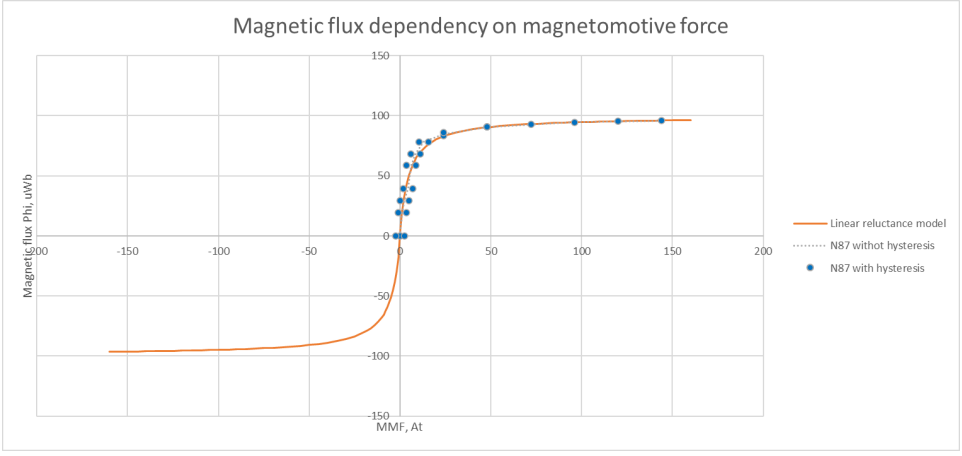


Figure 2.6. Dependency between magnetic flux and MMF in coupled inductor

The outcomes of the coupled inductor analysis have been combined in a single simulation model (Fig.2.7) that is used to as a digital twin of the multiphase converter with coupled inductor. The model has been verified by a direct comparison between simulation and experimental results, as depicted in (Fig. 2.8). The corresponding magnetomotive forces and magnetic fluxes in inductor cores, air paths and total flux are shown in (Fig. 2.9). Thereafter, the acquired simulation model is used to model the converter non-linear behaviour, reaction to ultimate operation conditions and analysis of the inductor saturation effects. An example inductor open circuit fault electric and magnetic parameters are shown in (Fig. 2.10).

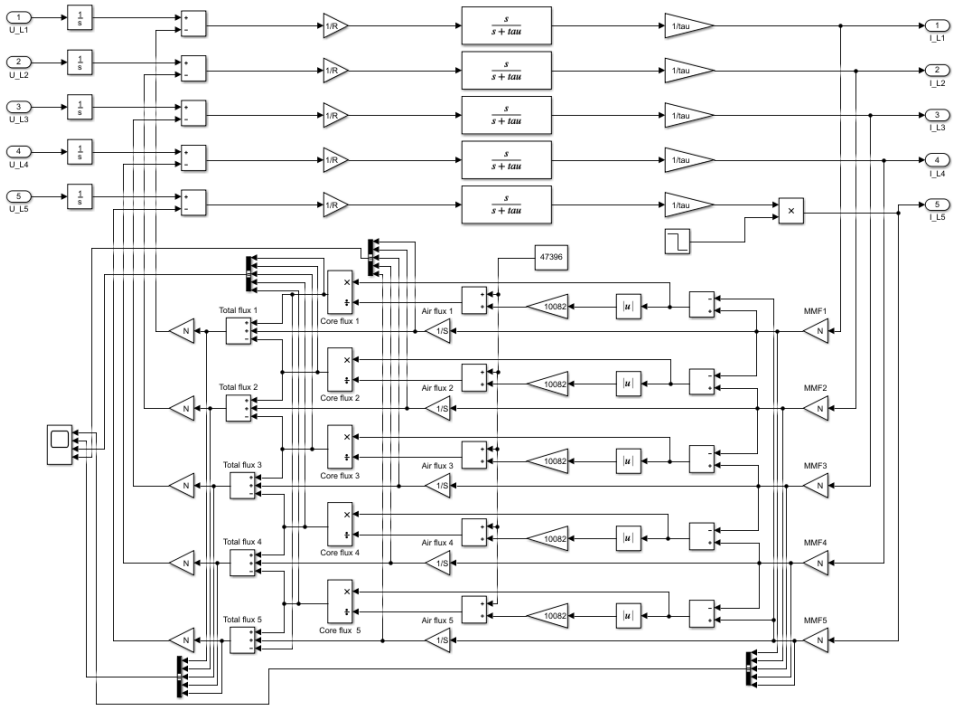


Figure 2.7. Non-linear simulation model of coupled inductor

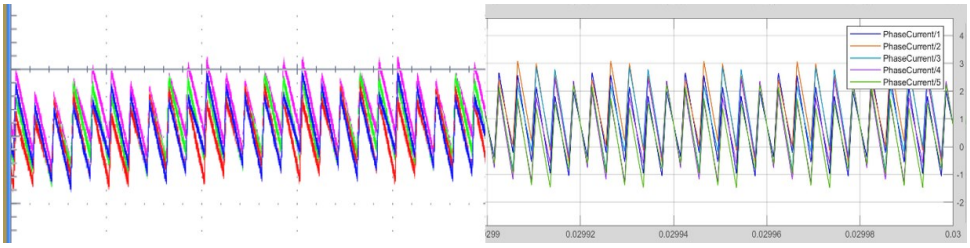


Figure 2.8. Non-linear simulation model of coupled inductor verification results: experimentally acquired phase currents (left) vs. simulated phase currents (right)

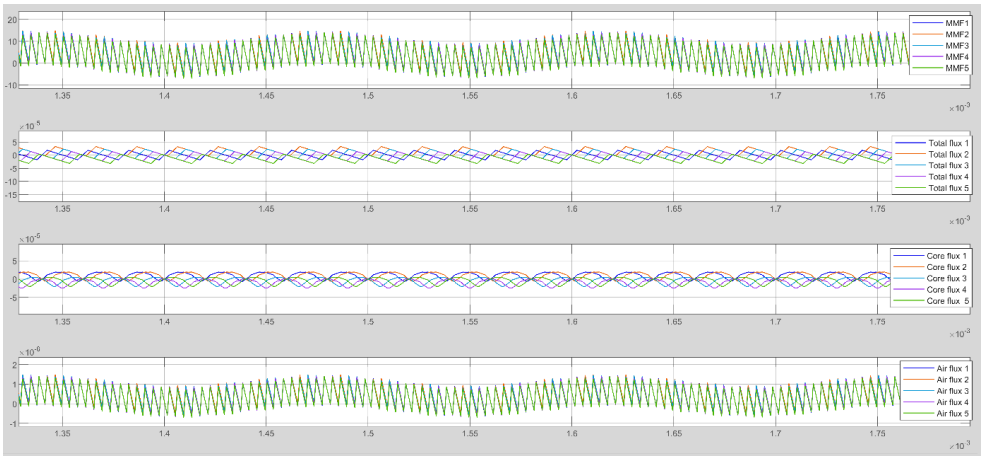


Figure 2.9. Non-linear simulation model of coupled inductor verification results: magnetic circuit parameters

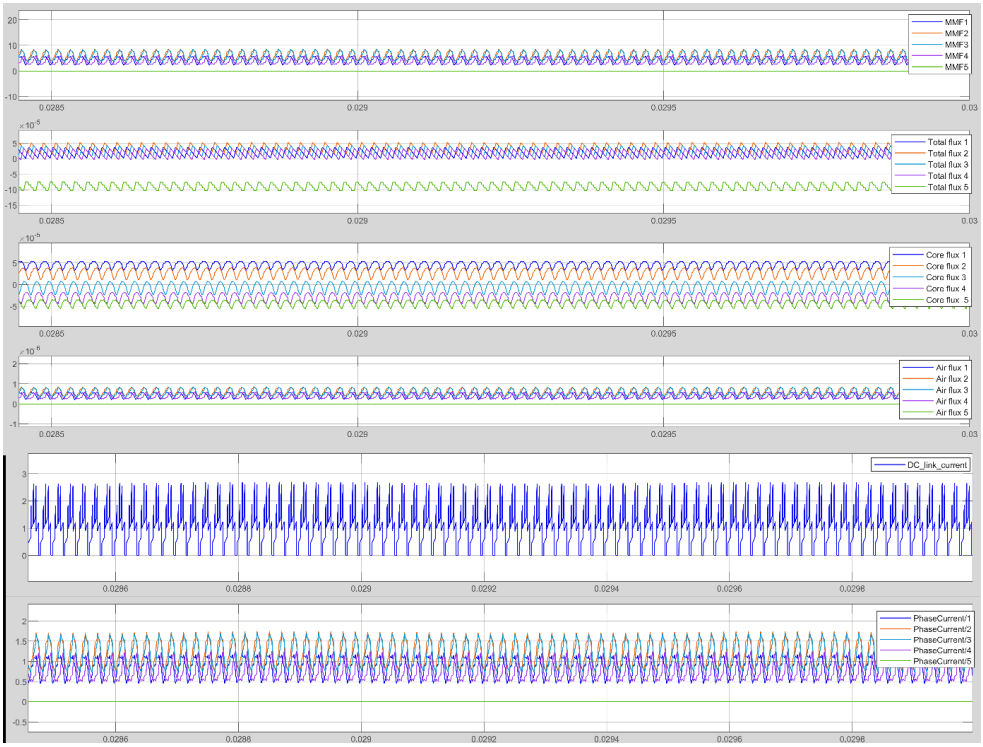


Figure 2.10. Simulated inductor open circuit fault electric and magnetic parameters

The dependency between converter duty cycle difference, current misbalance and converter efficiency is acquired experimentally and shown in (Fig. 2.11). Due to high coupling factor and

small leakage path, the DC component of magnetic flux is compensated in mutual inductor cores, if the phase currents and, hence, the fluxes in each core are equal [8]. Since even small change in inductor volt-second product causes phase current misbalance, the DC component of magnetic flux emerges and leads the core towards non-linear region and saturation. Once the coupled inductor core starts to operate in non-linear region, the hysteresis effect will intensify and cause increased core iron losses and, hence, lower efficiency of the converter. Moreover, the differences between phase currents are compensated by the equalizing currents flowing in the loops among phases and causing increased phase current rms values and, hence, winding copper losses due to the phases winding resistance. Nevertheless, the resistance of windings is small and not sufficient to limit the equalizing currents. Therefore, non-linear controller performance is required for effective current sharing among phases.

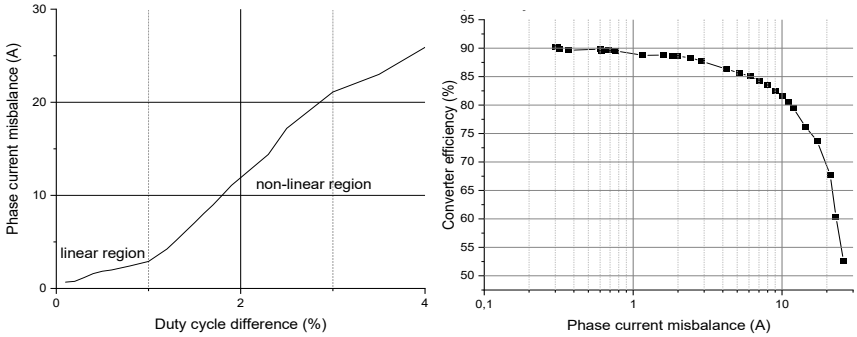


Figure 2.11. Dependency between converter duty cycle difference, current misbalance (left) and converter efficiency (right)

2.2. Fuzzy logic controller design

The current balancing controller is capable with both, current-mode and output voltage loop control with previously proposed [17]-[20] different control architectures, including error calculation based on average current, phase pair differences and master-slave topology. Error calculation based on average current is reasonable, when using current-mode control [17], because N controllers are required for a N-phase converter [20]. By calculating phase pair differences, only N-1 controllers are required for an N-phase converter [19], but in this case balancing controllers counteract each other and might disturb the outer voltage loop controller, hence, the full control decoupling is not achieved. In master-slave topology the master phase is regulated by outer voltage loop and slave phases are following the master phase current [20], thus, achieving full controller decoupling.

Different controller design techniques are known, including classical design in s-plane [10], [13], [20], state-space [19], [21], predictive [14] and non-linear [22] control. The classical controller design is limited by single input single output (SISO) system and often shows good performance at specific operational points [20]. State-space controller design can be considering multiple input multiple output (MIMO) system, which is advantageous, but still challenging for system with varying dynamics [19]. Predictive controller can achieve excellent

dynamic behaviour, but only if system parameters are well known [14]. Non-linear controller has significantly improved dynamic performance, but SISO system limits are still applicable [22]. For automotive auxiliary converter with high performance and fast response requirements, considering rapidly changing system dynamics, optimized controller parameters are needed [7]-[10], which cannot be fully achieved using previously described methods.

Fuzzy logic controller can combine the advantages of non-linear control for MIMO systems, ensuring high performance under varying system dynamics conditions [38]-[41]. Moreover, a classical PI (or PID) controller design for a multi-phase converter with coupled inductors can be very challenging due to complicated mathematical system description, non-linear behaviour of coupled inductors (hysteresis, saturation) and especially, at unpredictable load change conditions [38]-[41]. Fuzzy logic controller design requires just cognitive knowledge about the system behaviour and desired control logic [38]. As the controller input output variables and logic are fuzzified, the transitions between controller rules are smooth and control performance can be optimal in different operating conditions.

The control of converter with coupled inductor must consider the non-linear behaviour of the inductor cores, as described in previous subchapter 2.1. In addition to that, transient operation at the load change can show undesirable current balancing controller interventions, caused by misbalance due to incorrectly interpreted phase current value change that is a specific issue of single sensor current sharing schemes. The origin of this effect is illustrated by means of (Fig. 2.12). The load increase is shown with the gradually rising phase currents. The sample points of currents are distributed within the switching period, resulting in different values sampled due to the load change and not the misbalance. Nevertheless, a classical balancing controller would try to compensate these different current values and, thus, causing real phase current misbalance. To overcome these problems a fuzzy logic balancing controller is proposed for the auxiliary DC/DC converter control. An additional controller input variable “Load change” is introduced. The controller reaction speed will be adjusted depending on the load change rate. Hence, a reduced current balancing controller performance is proposed during transient with maximum performance applied at steady state. This control strategy will help to eliminate or at least reduce undesirable controller interventions.

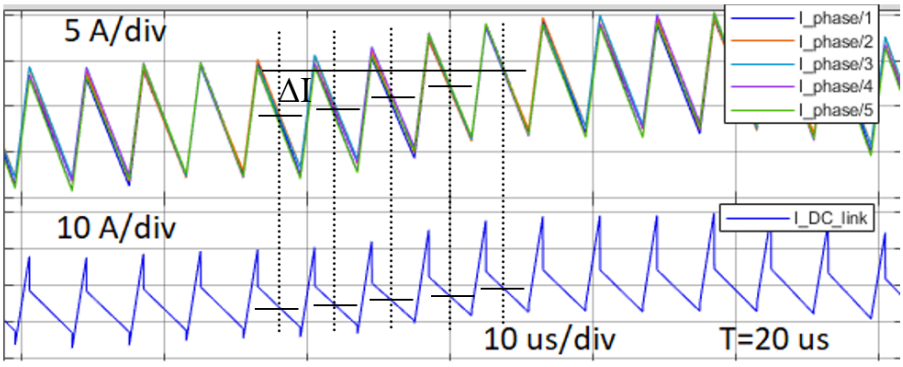


Figure 2.12. Converter operation at load change illustrating the pseudo-misbalance effect

Current balancing control architecture consists of DC link current measurement, phase current reconstruction, error and load change calculation, controller and PWM correction blocks, as depicted in (Fig. 2.13). An ICM technique with the following phase current reconstruction algorithms are used for phase current average value acquisition. When the phase current average values are obtained, errors are calculated by (2.9) independently on duty cycle range. The error calculation corresponds to master-slave topology, where phase 3 is chosen as a master and, hence, an average current in phase 3 is used as a reference value. Currents flowing in slave phases 1, 2, 4, and 5 are adjusted to a master phase 3. Difference equation (2.10) describes the calculation of the load change ΔI[n] using decoupled master phase 3 present $I_3[n]$ and past $I_3[n-1]$ current values.

$$\begin{bmatrix} e_{13} \\ e_{23} \\ e_{43} \\ e_{53} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \tag{2.9.}$$

where e_{ij} – error between the phase currents in i-slave phase and j-master phase, A;

I_i – current average value in i-phase, A.

$$\Delta I[n] = I_3[n] - I_3[n\text{-}1] \tag{2.10.}$$

where $\Delta I[n]$ – load current change, A;

$I_3[n]$ – actual current sample in master phase, A;

$I_3[n\text{-}1]$ – previous current sample in master phase, A.

4 identical fuzzy logic controllers are used in master slave current balancing control topology for a 5-phase converter with coupled inductors. Each controller processes fuzzified current misbalance and load change values at the input and returns a proportional and integral (PI) duty cycle correction at the output. The obtained duty cycle corrections are added to the main duty cycle from the output voltage controller and fed to the corresponding slave phase PWM module. The control architecture is shown in (Fig. 2.13).

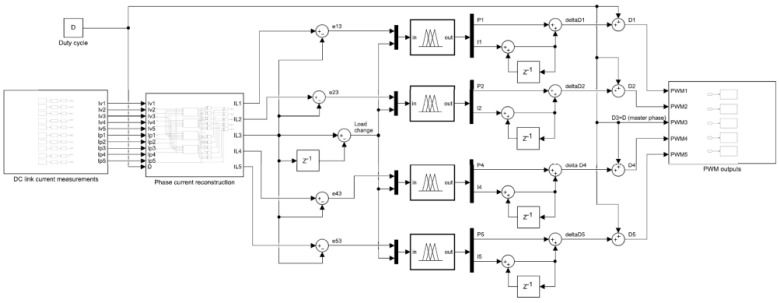


Figure 2.13. Current balancing control architecture with master-slave topology

Fuzzy logic controller is designed using Mamdani fuzzy interference system with triangular membership functions for both input (current misbalance and load change) and both output

(proportional and integral duty cycle correction) variables. A designed controller architecture with control surfaces for both outputs and 19 control rules are shown in (Fig. 2.14).

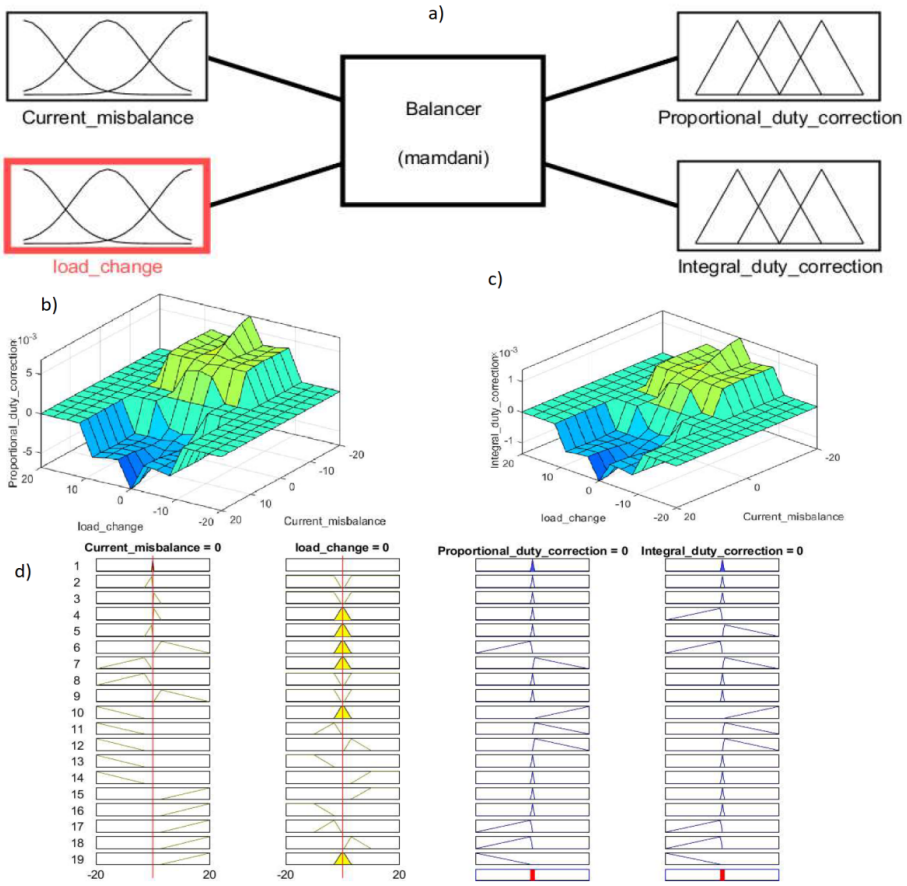


Figure 2.14. Fuzzy logic controller: a) architecture, b) proportional control surface, c) integral control surface, d) control rules

The maximum control performance will be achieved at steady state, when large phase current misbalance will occur. The proportional gain is intended to quickly compensate the suddenly emerged misbalance and designed, based on measured dependence between duty cycle difference and resulted phase current misbalance. A small integral part is added to compensate the steady-state error and ensure the reversion of magnetic flux DC component in inductor core to avoid saturation. During transients, the controller is operating with reduced performance to avoid undesirable interventions.

2.3. Control performance evaluation

The designed control concept has been validated by simulation and experimentally. Firstly, the comparison between the converter phase currents without and with the turned-on controller at steady state are shown in (Fig. 2.15). The converter was operated with duty cycle D=0.25 and duty cycle disturbance Δd=0.005, applied to phase 2 positive and phase 4 negative. The phase currents show obvious misbalance with non-linear waveforms, differing from simulation results without the control, but after switching the fuzzy logic current balancing controller on, equal phase currents with linear waveforms are observed in both cases.

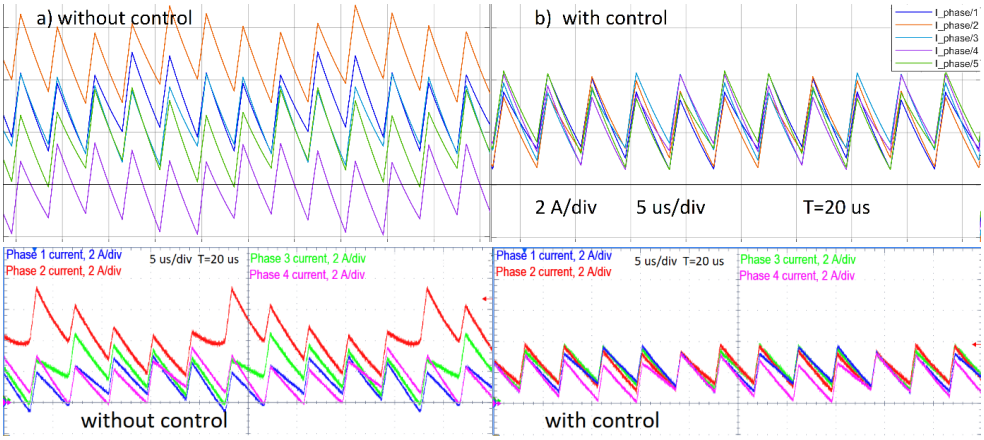


Figure 2.15. Simulation (top) and experimental (bottom) results for steady state: a) without and b) with current balancing control applied

To evaluate the controller performance during converter operation throughout the whole duty cycle range, phase current average values were measured. The measured phase current values depending on duty cycle in shown in (Fig. 2.16) with current balancing controller switched off and on, respectively. (Fig. 2.17) shows the resulting maximum current misbalance depending on duty cycle with and without control. It is observed from both measurement results that at each duty cycle phase current misbalance is large, when control is not applied. If controller is switched on, the current misbalance does not exceed 1 A of steady state error. These results correspond to accuracy limit of the ICM circuit, as described in [25]. Hence, it is possible to operate the converter within full duty cycle range with small current misbalance, without causing considerable efficiency degradation or inductor core saturation.

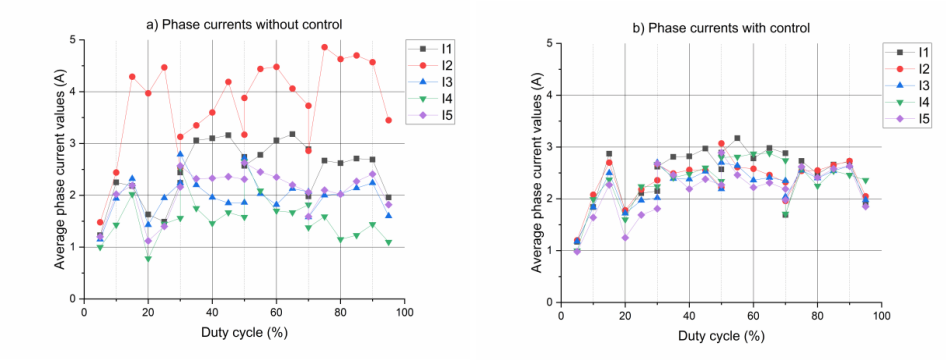


Figure 2.16. Experimentally measured phase current values depending on duty cycle: a)without and b)with current balancing control at steady state

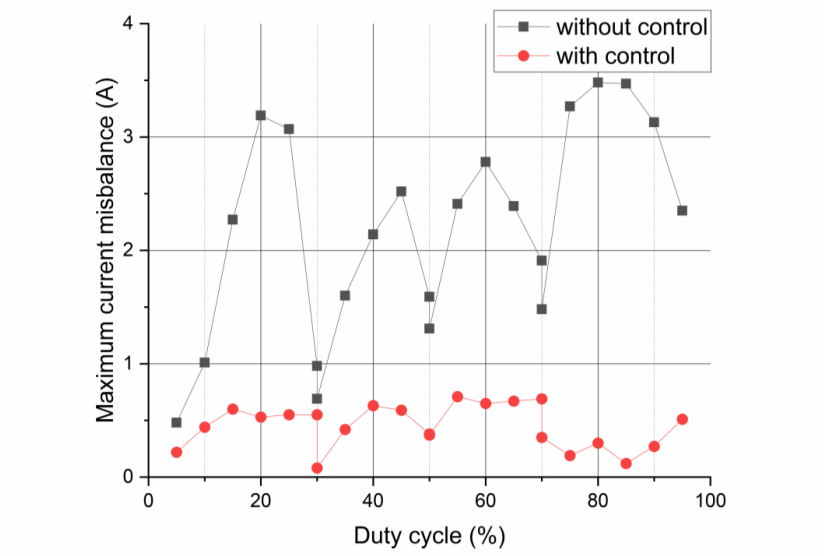


Figure 2.17. Resulting maximum current misbalance depending on duty cycle with and without current balancing control at steady state

The step response of phase current balancing controller has been acquired from simulation and experimental verification and is shown by means of phase current waveforms at controller turn-on in (Fig. 2.18). The current balancing control can achieve nearly zero steady state error within 1 ms after controller turn-on, with higher gain initially when prototype converter currents showed stronger misbalance due to core saturation, and lower gain in the linear region.

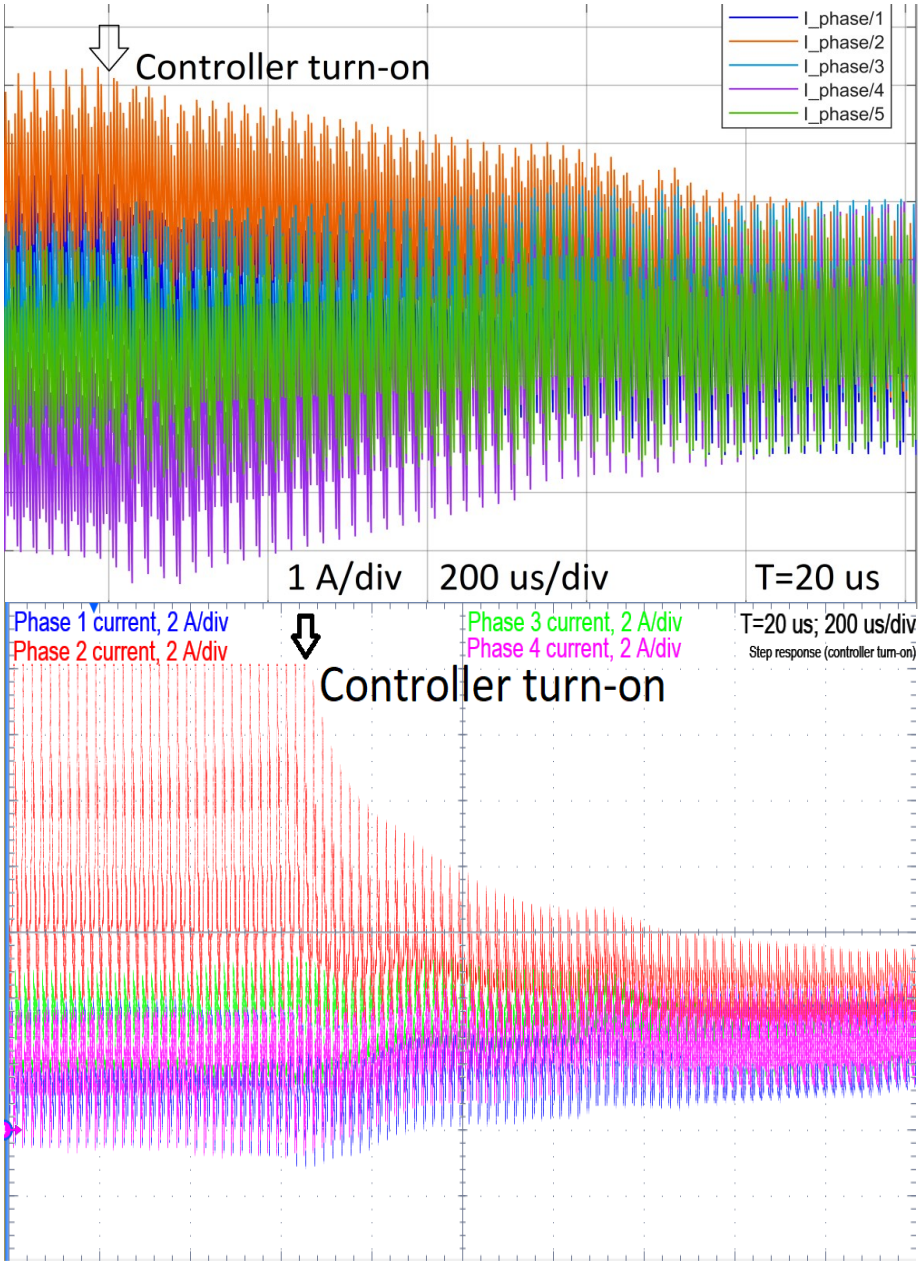


Figure 2.18. Current balancing controller step response at turn-on: simulation (top) and experimental (bottom) results

The phase current waveforms under load current increase conditions are shown in (Fig. 2.19) a) and b) without and with load change input variable enabled, respectively. Thus, an influence of load change algorithm on the control performance can be analysed. Significant

undesired current balancing control interventions can be observed on phase current waveforms, when load change variable is disabled and smooth waveforms are observed, when the load change algorithm is enabled. The phase current waveforms under load current decrease conditions are shown in (Fig. 2.20). A smooth phase current decrease without any undesired interventions can be observed.

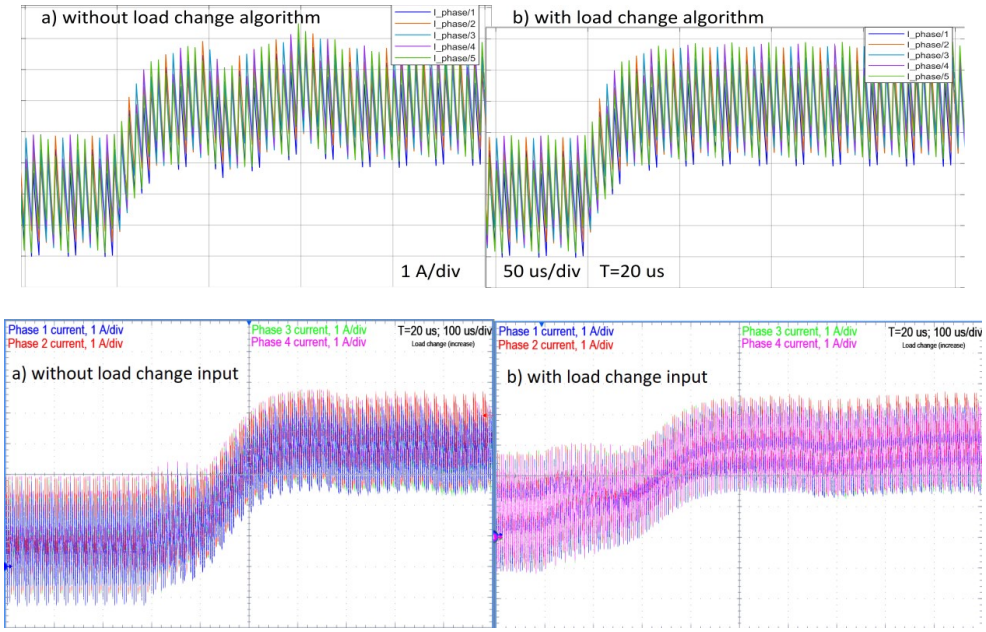


Figure 2.19. Phase currents at load change: simulation (top) and experimental (bottom) results for cases a) without and b) with enabled load change algorithm

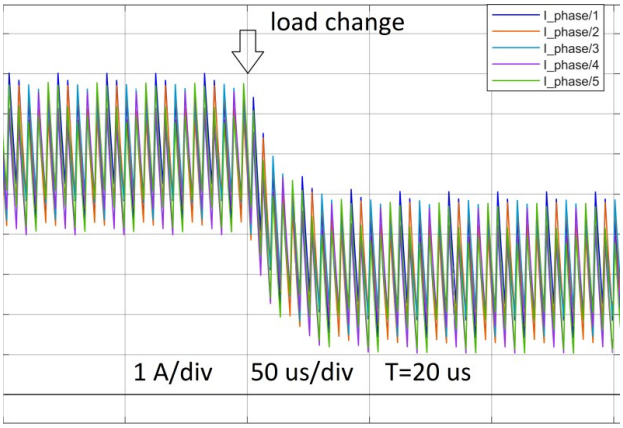


Figure 2.20. Simulated phase current waveforms at load current decrease

Finally, the sinusoidal duty cycle disturbance is applied to measure the controller frequency response. The sinusoidal duty cycle disturbance $\Delta d=0.005$ with frequency ranging from 1 Hz

to 10 kHz was applied to phases 2 and 4 in opposite directions, to determine the open loop (converter) and closed loop (controller) system reaction to slow and fast disturbances. The resultant open loop and closed loop current waveforms are shown in (Fig. 2.20). The frequency response for the open and closed loop systems is shown in (Fig. 2.21). The open loop system reaction on slow disturbances is large, but it decreases for faster disturbances. On the other hand, the closed loop system reaction on slow disturbances is very small, but it gradually increases, when disturbance gets faster. Hence, the controller achieves maximum performance on low frequencies and at high frequencies the control performance is minimal.

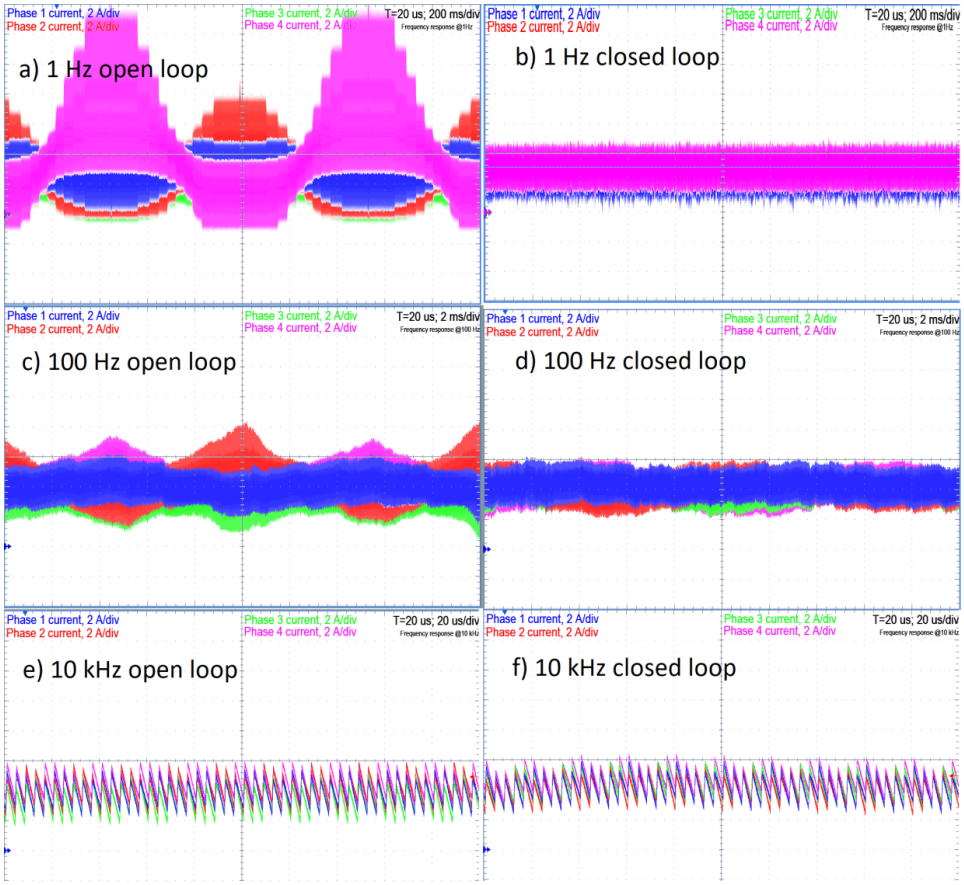


Figure 2.20. Phase current waveforms under sinusoidal disturbance conditions: a) open loop @ 1 Hz, b) closed loop @ 1 Hz, c) open loop @ 100 Hz, d) closed loop @ 100 Hz, e) open loop @ 10 kHz, f) closed loop @ 10 kHz

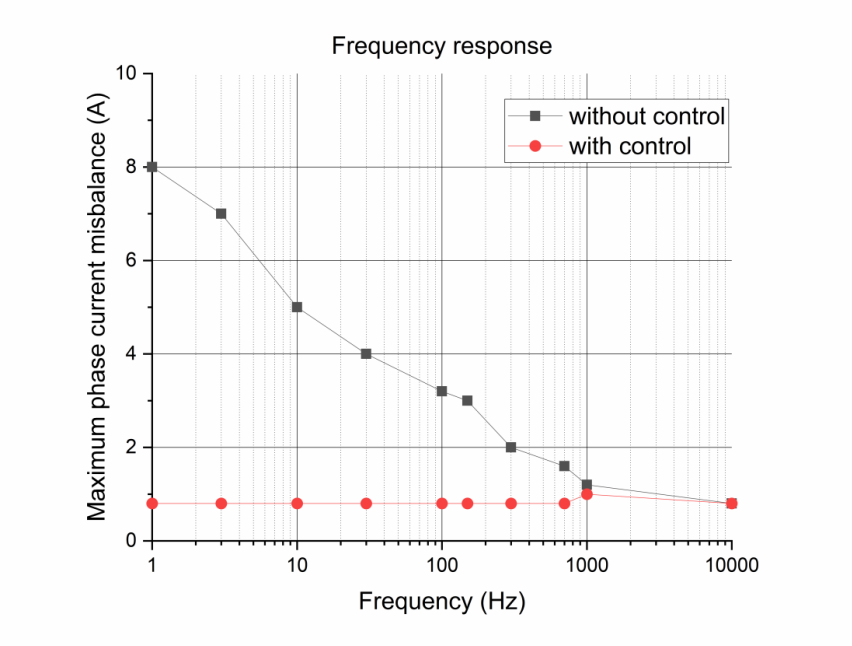


Figure 2.21. Frequency response on the current misbalance for the open and closed loop

As the real current misbalance causing factors are slow and change gradually with time [10], the obtained controller behaviour corresponds to the necessary requirements and, hence, the aim of specific variable current balancing controller performance is achieved. Moreover, a sufficient current balancing controller steady state behaviour is observed within the full converter operation range.

2.4. Conclusions

Multiphase converter with coupled inductor demonstrates a non-linear behaviour due to the possible core saturation, caused by the current misbalance and resulting magnetic flux DC component. Using single sensor ICM technique can cause undesired current balancing controller interventions during the load change. Application of fuzzy logic under these circumstances allows to design a non-linear complicated controller in relatively easy and intuitive manner, by measuring the open loop system parameters and applying the cognitive knowledge about the system. As a result, the desired closed loop system behaviour is achieved.

Simulation and experimental results show good current balancing controller performance at steady state with low steady state error, caused mainly by indirect DC link current measurement circuit accuracy limits. The remaining phase current misbalance is low and cannot cause significant efficiency decrease. Experimental results showed only linear current waveforms, when the control is enabled, and, hence, no inductor core saturation or converter failure can be expected.

The current balancing controller dynamic behaviour was designed to achieve high performance at low frequencies and reduced performance at high frequencies or under fast load change conditions. An enhanced transient behaviour was achieved by implementing a fuzzy logic controller with non-linear gains and considering the load change rate as an additional controller input variable. The resulting transient responses are validated using simulation and experimental results, by evaluating the transient operation under load change conditions, step response at controller turn-on, and the frequency response on sinusoidal disturbance. Obtained phase current waveforms fully meet the necessary current balancing control requirements and, hence, the aim of an optimized current balancing controller behaviour is achieved.

3. FAULT DETECTION AND FAULT TOLERANCE

Auxiliary converter system provides power supply for safety critical systems. As the failure in power supply may lead to catastrophic consequences, the fault detection and fault tolerant operation is required to ensure reliable uninterruptible power supply. This chapter introduces the converter ICM based fault detection and identification method and describes the fault tolerant operation algorithm for uninterruptible operation even with active fault.

3.1. Fault detection and identification

As described in the previous chapters, the phase current values can be obtained by means of ICM and used for current mode control or balancing controller implementation, which in both cases will protect the converter from excessive equalizing currents and resulting core saturation and efficiency decrease under normal operating conditions. However, the converter circuit elements, such as semiconductor devices, inductors and capacitors can fail randomly or under certain circumstances [42]. Parts with the highest stress and thermal loads have the highest failure probability [42]. In an automotive bi-directional converter, the MOSFETs have the highest failure risk, resulted by the switch, remaining on short or open circuit state in converter single or multiple phases [42]-[44]. In this case a failure in one or more phases will not lead to the whole converter refusal and, hence, it is essential to determine and locate the fault as quickly as possible, to protect the converter from further damage and ensure at least uninterruptable power conversion with reduced power for high priority loads.

The DC link current waveforms are therefore analysed in terms of failure condition reflection. The ICM technique is used to detect the overall fault conditions and specify the failed component. Fault detection performance is assessed, considering fault type and time, necessary for detection. The detected faults can then be used to take specific actions or implement the converter fault tolerant operation algorithms, thus, ensuring higher reliability.

The main distinguishing criteria of normal current misbalance condition is slow appearance and obvious response on current balancing controller interventions. Fault conditions, in opposite, appear suddenly, cause rapid current changes and do not react on controller caused duty cycle corrections. Hence, the fault detection must mainly rely on current change rate dI/dt. This is especially important in case of short circuit in semiconductor switch. Short circuits are rare, but harmful events [42], causing rapid current rise limited by relatively small parasitic inductances, when both half-bridge switches are closed. Therefore, the short circuit detection must be performed very fast. This can be done by using multiple distributed DC link current measurements within a switching period. Open circuit faults can happen with higher probability but have significantly lower risks of causing permanent converter damage [42]. Nevertheless, open circuit faults must be detected to avoid the rise of equalizing currents, causing coupled inductor saturation. It is generally more challenging to detect open circuit, as it is not always leading to rapid current changes. Hence, the secondary criteria of no reaction on current balancing controller interventions can be used.

Fault detection is based on the reconstructed phase currents from the ICM samples. Phase current average values and their change rates are used for the fault type identification. The overall converter control structure with the failure diagnosis module is depicted by means of a block diagram in (Fig. 3.1). It is assumed, that only one fault may appear at once, as the probability of multiple faults appearing at the same time is low [42] and it is very likely, that the case of multiple faults is caused by a serious converter failure, that will not allow fault tolerant operation. The possible converter semiconductor switch faults and their conditions for identification are listed in (table 3.1). The listed conditions are then used for converter control in the "Fault detection" subsystem in (Fig. 3.1).

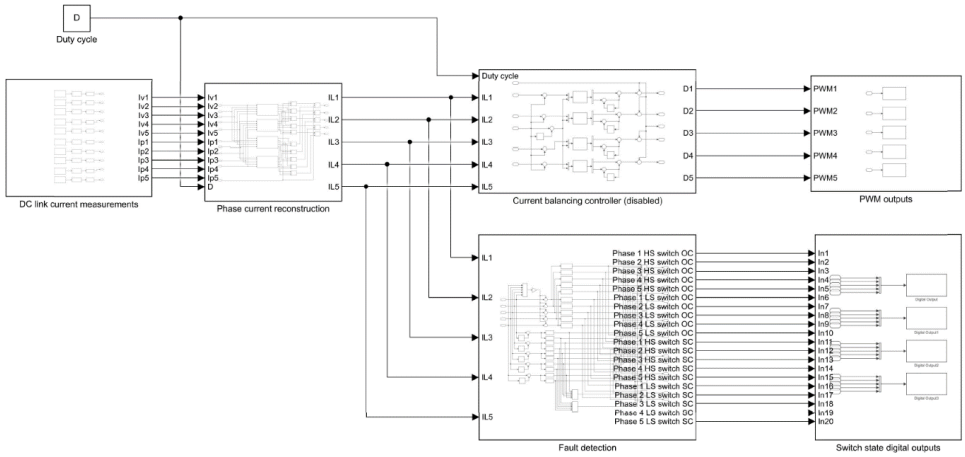


Figure 3.1. Block diagram of the overall converter control structure including the failure diagnosis module

Table 3.1.

Possible converter switch faults and their identification conditions

Possible fault description	Identification conditions		
	Phase current actual value	Current change rate	Current change rate in all phases
High side switch open circuit 1 phase	below average	fall in affected phase	no fall
High side switch short circuit 1 phase		rise in the rest phases	no rise
Low side switch open circuit 1 phase	above average	fall in the rest phases	no fall
Low side switch short circuit 1 phase		rise in affected phase	no rise

The simulation results for a typical open circuit fault case in one converter phase is shown in (Fig. 3.2) by means of phase and DC link currents, as well as the coupled inductor magnetic circuit parameters. The phase currents in (Fig. 3.2) depict the case when an open circuit happens in phase 5. The magnetomotive forces corresponding to the phase currents follow the phase current patterns. This causes a rise in DC component in the cores of coupled inductor until the partial saturation followed by phase current ripple rise is observed. The DC link current waveforms reflect these changes and at specific time points it shows values equal to zero.

Hence, the DC link current waveforms reflect active failure conditions and this property can be used to detect failures.

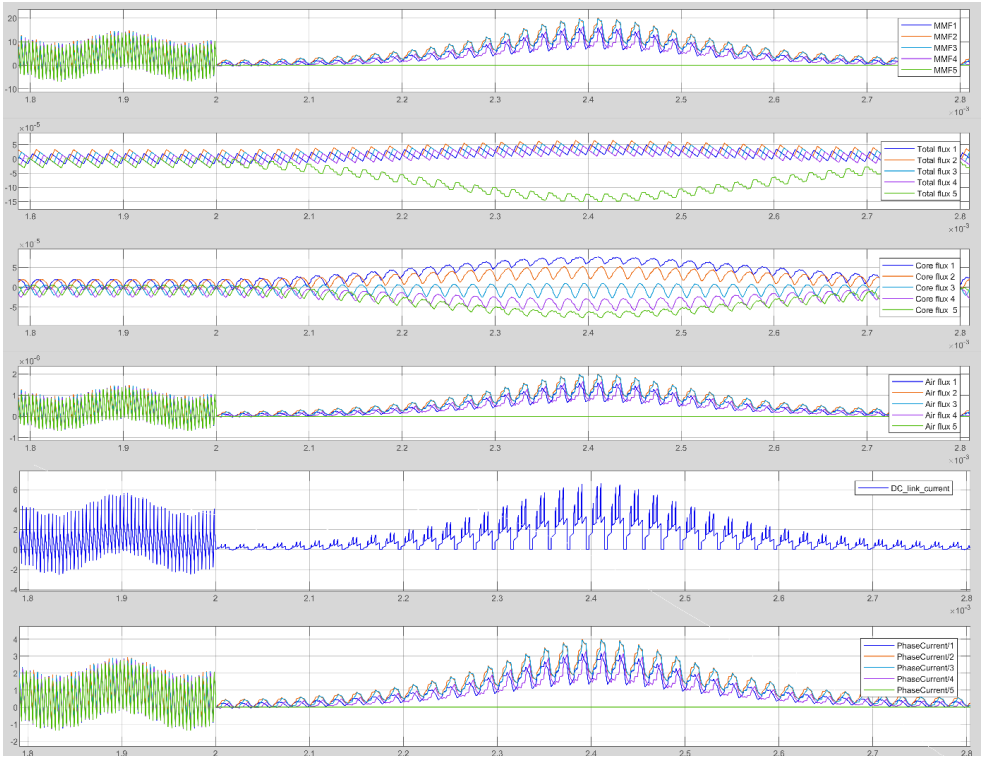


Figure 3.2. Simulation results of open circuit fault in one converter phase

Further analysis of failure conditions is performed experimentally. The experimental results for 4 typical fault cases, i.e., high side and low side switch open and short circuit, are shown in (Fig. 3.3). In both cases the open circuit (a) and short circuit (b) conditions are shown with the corresponding digital signal representing health state, that is high for no fault and low for the corresponding fault condition.

Analysis of (Fig.3.3) shows that any of the high side switch faults will cause a corresponding DC link current measurement, linked to a failed phase current value, rapid decrease. In case of open circuit, the corresponding phase current value drops, but in case of short circuit, the phase current is not influenced strong enough to detect the fault using direct measurements. This is resulted from the condition, when both switches are closed, causing the short circuit in DC link. Nevertheless, the ICM waveforms reflect the existing fault condition. Any of the low side switch faults will cause a corresponding DC link current measurement, linked to a failed phase current value, rapid increase. In case of open circuit, the corresponding phase current value rises mostly due to the resulting discontinuous conduction mode, but the phase current is flowing through the body diode. In case of short circuit, the phase current rise

is not significant. However, the ICM waveforms reflect the existing fault conditions in both cases better, then the phase currents would do.

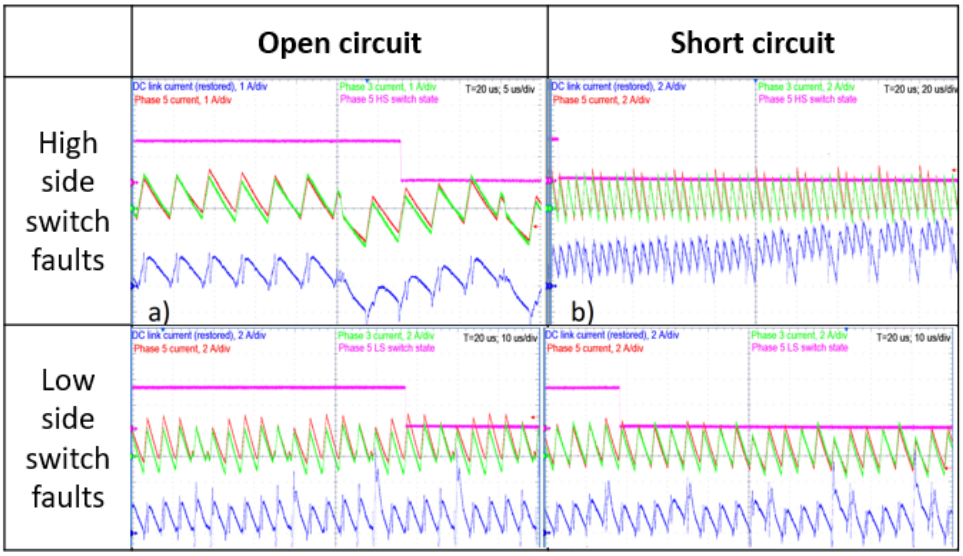


Figure 3.3. Current waveforms, reflecting the specific semiconductor switch faults

The relationship between phase and DC link current depends on the duty cycle. Therefore, there are 4 different phase current reconstruction algorithms derived in subchapter 1.2. As the DC link current waveforms in a 5-phase converter differ in the duty cycle ranges D<0.4, 0.2<D<0.6, 0.4<D<0.8 and D<0.6, the fault detection and identification performance might also be influenced by these differences. Hence, a verification of fault detection method is necessary in all 4 duty cycle ranges. This has been done for the same high side switch open and short circuit cases at D=0.25, D=0.4, D=0.6 and D=0.75. The corresponding high side switch states, the phase and ICS waveforms for open and short circuit cases are shown in (Fig. 3.4).

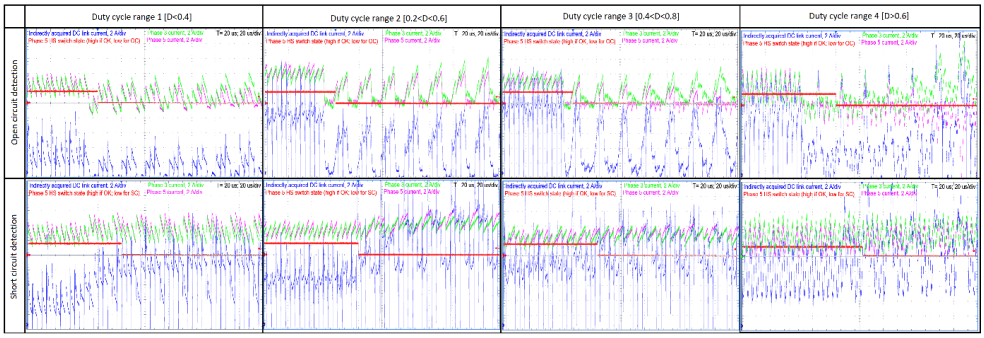


Figure 3.4. Fault detection results for different duty cycle ranges

Analysis results in fact that application of the different current reconstruction algorithms, depending on duty cycle ranges does not have any impact on the fault detection performance. The disturbing factors for fault detection performance might be converter transients and pseudo-fault detection. Converter transient might be caused by sudden load change or rapid input voltage drops. This might lead to pseudo-fault detection when the converter operation is still normal. To overcome this effect, fault detection and identification algorithm includes an additional conditional statement, ensuring, that the current change is not happening in all phases at the same time. Thus, converter transients, when currents can change rapidly, are not being interpreted by the algorithm as failure. Another pseudo-fault event might happen shortly after the single fault detection event. Especially at short circuit, the converter currents can be exposed to very rapid changes, that might be interpreted by the algorithm as another independent fault event. This drawback can be eliminated only partially, by checking conditional statement, ensuring, that the current change is happening only in affected phase or in the rest phases at the same time. This gives the controller an adequate timeframe for reaction and enabling the fault tolerant operation algorithms. The corresponding switch states and current waveforms during transient and single phase fault is shown in (Fig. 3.5). The switch states in (Fig. 3.5) show, that no pseudo-fault events are generated at transient and at least 250 us after the single-phase fault event. Hence, the proposed method is reliable enough.

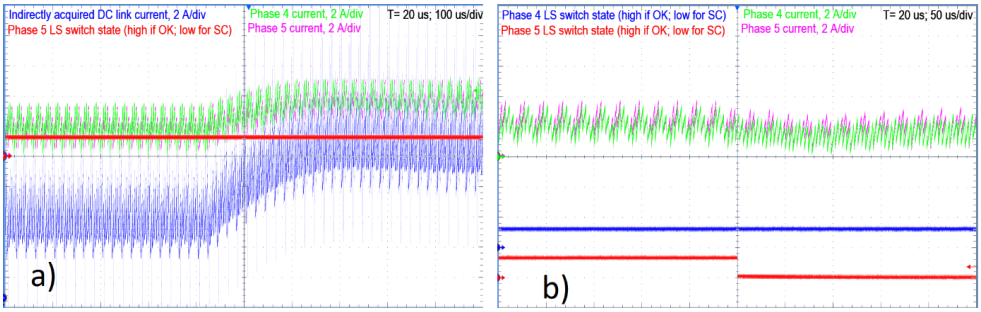


Figure 3.5. Switch states and current waveforms during a) transient, b) single phase fault

Finally, the fault detection time measurements have been performed to assess the fault detection performance at different converter operating points within the whole duty cycle range. The resulting graph in (Fig. 3.6) verifies that the fault state can be detected within 10 to 20 us in case of open circuit and less than 4 us in case of short circuit within the whole converter duty cycle range. The switch state estimation utilizes the current change rate and current misbalance evaluation. Hence, the short circuit condition can be detected faster, because of higher change rate. Open circuit conditions are generally slower and, therefore, need more time for detection and identification. After detection of the failed switch as further described in [45], the corresponding phase can be deactivated to allow the converter fault-tolerant operation with reduced number of phases [46]. Hence, the converter can be operated with reduced performance, but will not fail completely, thus, ensuring higher energy conversion reliability.

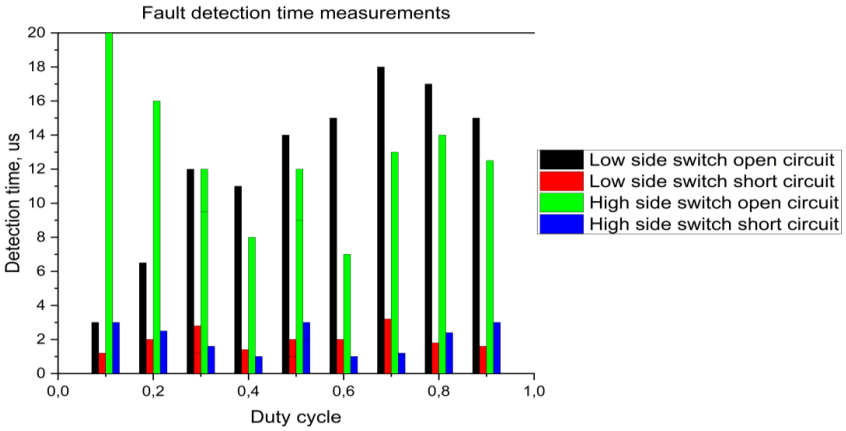


Figure 3.6. Fault detection time measurements at different converter operation points

3.2. Fault tolerance

Reliability plays an important role in modern power electronic system design. Recently a concept of Design for Reliability has gained an increased interest for ensuring more reliable and fail-safe field operation of power electronic converters by implementing reliability assessment based on Physics of Failures already at the design stage [47], [48], that is especially important in automotive application [49]. Complete assessment of power electronic system physics of failures requires knowledge about power semiconductors, passive components, control electronics, communication systems and software wear-out functions, including modeling of thermal cycling, humidity, vibration and other stressors [48]-[50]. Hence, there is a need for multi-physical modelling of power electronic component degradation for implementing Design for Reliability [47] with continuous improvements based on field operation data from health management and condition monitoring systems [50]. Current state of the art provides comprehensive knowledge about silicon semiconductor devices wear-out and short circuit failure mechanisms, based on thermal cycling model [48], as well as the capacitor degradation and failure models [49]. However, there is still lack of knowledge about different other components (e.g., PCBs, interconnects, cooling systems, etc.) and stress factors (e.g., humidity, vibration, shock, etc.) [49]. Consequently, it makes reliability-oriented design of magnetic components challenging [48] in case of multiphase converter with coupled inductors. Therefore, the use of fault-tolerance concept can be considered to improve and complement the reliability-oriented design, by filling the existing gaps in the knowledge and provide fail-safe fault-tolerant operation instead of converter component redundancy.

Fault-tolerance is a key aspect to enhance the power electronic system reliability. Although the reliability-oriented design and health management systems for power electronic converters can ensure extremely low probability of failures, a lot of research must be conducted on different component degradation mechanisms to minimize the risks of different possible failures [48]-[50]. At some applications (e.g., automotive advanced driver assistance and other

auxiliary safety-critical systems) black-out of power supply is not an option, due to high risks of catastrophic consequences, even if the probability of failures is minimized [51]. In this case a system must be able to continue performing its intended function despite the failure [50], or at least provide emergency operation with reduced performance to fulfil the requirements of functional safety [42], as by definition of fault-tolerance. Moreover, the fault tolerant operation can replace the high level of system redundancy, e.g., by using multiphase machines instead of redundant 3-phase machines in safety critical drive systems [50]. Similarly, the multiphase design of power electronic converters with fault-tolerant operation algorithm can meet the high standards of functional safety and reduce the component redundancy. Hence, the development of fault-tolerant operation algorithms is essential to provide uninterruptable power supply for safety-critical applications.

Different fault-tolerant operation technics were proposed recently for power electronics systems. A monolithic single-phase integrated circuit with fault detection and switch blocking capabilities is proposed in [51] to ensure fault-tolerance in multiphase hybrid Dickson converter for safety-critical applications. In [52] an additional inverter leg with 4 switches is added to a 3-phase inverter to provide fault-tolerant operation of an electric vehicle drive. In [53] the existing buck / buck-boost converter topology is modified with 3 additional switches to provide fault-tolerant PV system operation. A boost converter with additional parallel low-side switch is proposed in [54], thus, achieving low side switch interleaved operation in normal mode and single-phase operation in case of low-side switch open circuit fault. Similarly, a unidirectional interleaved 3-phase boost converter with additional fuses is used for isolation of a faulty phase and ensure fault-tolerant operation with reduced number of phases [55]. Hence, in the most cases additional components are used for redundancy and in case of faults the power flow is distributed between the remaining components. Though, it is an indicator of not optimal component utilization in normal operation (healthy) mode.

Fault-tolerant operation and reliability of bidirectional multiphase interleaved buck converters was investigated recently and showed good results. Operation of a 4-phase converter with deactivated phases was investigated in [43] and showed possibility of coupled ladder type core saturation without power loss increase. A partially decentralized control algorithm with PWM carrier phase-shift re-configuration was proposed in [56] and achieved operation with stable output voltage in case of 4-phase converter with uncoupled inductors and multiple current sensors. Fault tolerant single-phase operation of a 2-phase converter with none, weak and strong coupling was investigated in [57], achieving better results for the case of weakly-coupled inductors. Reliability indicator comparison is presented in [43], showing the benefits of coupled inductor converters over uncoupled inductor multiphase and single-phase buck converters. Hence, the multiphase interleaved buck converter topology utilizing coupled inductors has advantages in terms of reliability, fault-tolerance, and ability to provide fail-safe operation in safety-critical applications.

The proposed fault-tolerant operation algorithm is initiated in case of an active fault in any of the converter legs. Firstly, the corresponding phase leg with an active fault is being shut down to avoid any damage, caused by the fault. In the case of active faults in multiple phases, all the affected phase legs are switched off. Thereafter, for the remaining in operation phases

with healthy states, the PWM carrier phase shifts are re-distributed between each other with equal phase shifts, as expressed by (3.1). As a result of a single fault, converter continues operation with one deactivated phase, as it would be in a normal 4-phase converter operation. Or in the case of active faults in multiple phases, more phases are deactivated for 3 or less-phase mode.

$$\Delta T_i = \frac{T}{n} \tag{3.1.}$$

where ΔT_i – phase shift between PWM carriers, s;

T – switching period, s;

n – number of phases remaining in healthy state.

To ensure the converter operation with reduced number of phases, the fault-tolerant operation algorithm is integrated into the overall converter control algorithm, as shown in (Fig. 3.7) by means of the corresponding flow chart. The overall converter control algorithm consists of 3 paths - main path, control path and fault-tolerant path. The main path is initiated in any case by generating PWM outputs, sampling indirect DC link current, phase current reconstruction and fault condition monitoring. If no reset or shutdown is requested and there is no active fault, the control path is proceeded sequentially. The control path consists of the duty cycle corrections by the inner current balancing controller and the main duty cycle calculation by the outer voltage control loop with returning to the main path. If a new active fault state is detected by the end of the main path, the fault-tolerant path is proceeded. The fault-tolerant path follows the faulty phase shutdown, PWM carrier re-distribution and enabling the state of fault-tolerant algorithm (setting to 'true'). If the reset or shutdown is requested, the main program returns to the end, but at the start, the control mode is being reset to the normal mode with all phases being activated. Hence, the fault condition is cleared by each reset and algorithm will need to make 1 full cycle (equivalent to 1 switching period) to switch back to the fault-tolerant mode, if any active fault persists.

The proposed fault-tolerant operation algorithm is intended to avoid the converter shutdown and provide an effective solution for converter operation with optimal performance in case of most common converter faults. It is supposed to be initialized in case of faults caused by transistor, gate driver or inductor winding open circuits. However, the use of the proposed algorithm is limited, if semiconductor switch short circuits or other rare, but harmful events appear. The possibility of rare events is low, nevertheless, another set of measures must be undertaken to negotiate potential harm from this type of failures. The converter protection from short circuits is not covered by the proposed fault-tolerant operation algorithm. Nevertheless, it can be realized using the existing gate driver protection functions, resulting in the corresponding switch open circuit, that would allow to use the proposed algorithm and avoid the complete converter undesired shutdown.

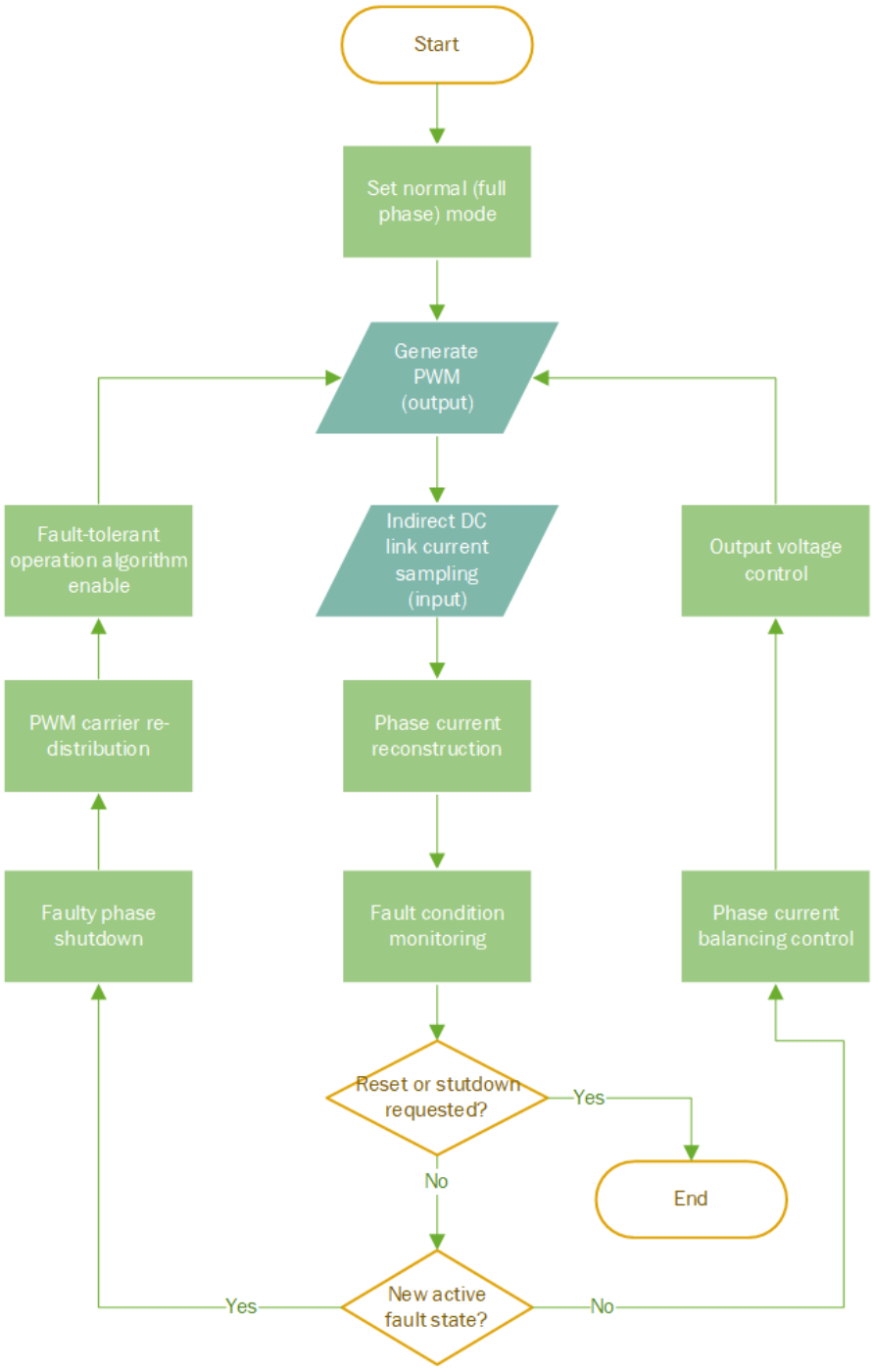


Figure 3.7. Flow chart of the overall converter control with integrated fault-tolerant operation algorithm

For the experimental verification of the fault-tolerant operation algorithm, the fault conditions are modelled intentionally. A switch open circuit event is generated by shortening the corresponding gate driver input. Inductor fault is generated by a separate switch, causing an open circuit fault in phase 5. The converter control algorithm is equipped with an additional external input signal for switching on or off the fault tolerant algorithm part. Hence, the converter can be operated in different modes – in normal (healthy state) with all 5 active phases, with an active fault in 1 or multiple phases without transition to fault-tolerant algorithm or with automatic transition to fault-tolerant algorithm. Thus, both, steady state and transient operation can be evaluated in different modes. The comparison between different mode steady state operation under high load is shown in (Fig. 3.8). Although all converter phases were in operation, (Fig. 3.8) shows only phase 1, 4 and 5 currents for the sake of simplicity and better overview. The experimental results show that at steady state the fault-tolerant operation algorithm minimizes the negative effects of an active open-circuit fault and converter can perform its functions with optimal performance. Under high load conditions the phase currents show high peaks, caused by inductor partial saturation due to an active fault. The transition to fault-tolerant operation reduces the current peak and, hence, the inductor saturation effects significantly, thus, allowing operation with much better performance.

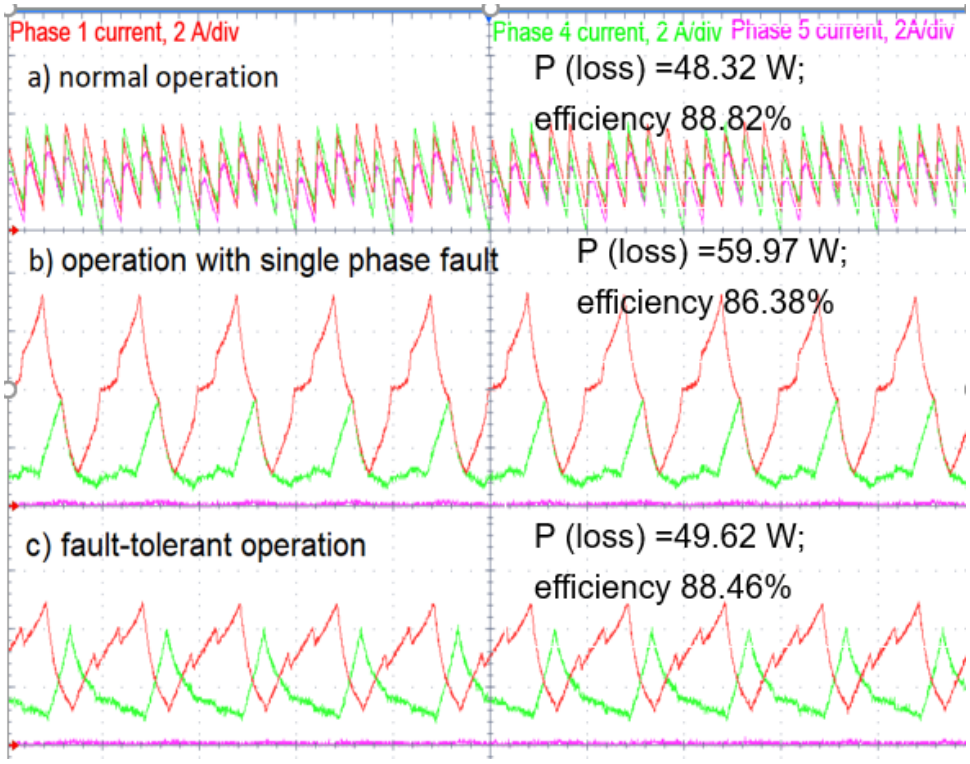


Figure 3.8. The compassion between different mode steady state operation

The comparison between separate phase and total currents in different steady state operation modes with moderate load is shown in (Fig. 3.9) by means of separate phase currents and their sum. Similar results are acquired by the moderate load. As the inductor saturation effects are not observed under the active fault condition, the performance improvement has smaller effect. Nevertheless, the fault-tolerant operation results show the reduction of phase and total current rms values, current ripples, total loss power and improved efficiency in comparison with operation with active fault and switched off fault-tolerant algorithm.

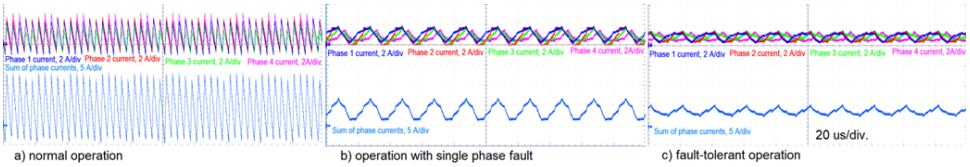


Figure 3.9. The comparison between phase and total currents in different steady state operation modes

The measured voltages and currents at converter input and output ports is shown in (Fig. 3.10). The resulted numerical values with calculated power of loss and efficiencies for all operation modes are listed in (table 3.2). In normal 5-phase operation with duty cycle of 25% the currents show higher ripples in comparison with 4-phase operation, where ripples are compensated by inductor coupling. This is caused by relatively large influence of switching frequency 5th harmonic on the total current in normal operation. In case of fault-tolerant operation in 4-phase mode, the switching frequency 4th harmonic influence on total current is reduced due to more favourable PWM carrier phase shift re-configuration. Nevertheless, the switching frequency component is present due to different pulse delays through the drivers and imbalances in the core, that can be further optimized by e.g., implementing the active phase-shift control described in [52]. Consequently, due to the increased coupled inductor hysteresis (iron) losses, the converter efficiency decrease is observed in case of operation with active fault. Due to transition to fault-tolerant operation, the efficiency decrease is being reduced.

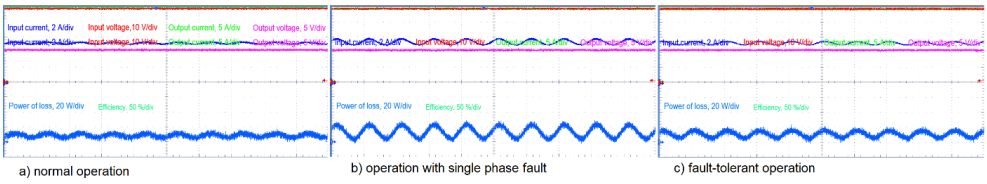


Figure 3.10. The comparison between measured voltages and currents at converter input and output ports in different steady state operation modes

Hence, the proposed fault-tolerant algorithm allows further converter operation with active fault, minimizes current ripples, and optimizes converter performance with significant improvements under high load conditions. Under moderate load conditions the converter performance is improved by the proposed fault-tolerant operation algorithm, however, it can be

further optimized by implementing additional phase-shift control to compensate the core imbalances, thus, achieving even better performance.

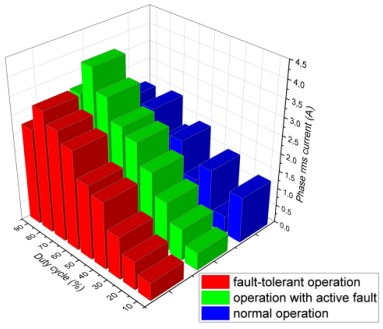
Table 3.2.

Comparison between converter parameter numerical values in different operation modes

Parameters	normal operation	operation with active fault	fault-tolerant operation
Phase rms current, A	1.1	1.3	1
Phase current ripple, A	3.9	1.9	1.2
Total rms current, A	5.5	3.8	3.9
Total current ripple, A	16.9	6.3	4
Power of losses, W	9.9	13.9	11.2
Efficiency, %	92.5	88.9	91.7

Converter steady state operation has been verified in full duty cycle range. The comparison between current rms and ripple value measurements are presented for normal operation, operation with single phase fault and fault-tolerant operation. Phase current and total current rms values are shown for 3 different modes in (Fig. 3.11). Phase current maximum ripple and total current ripple values are shown for 3 different modes in (Fig. 3.12).

a)



b)

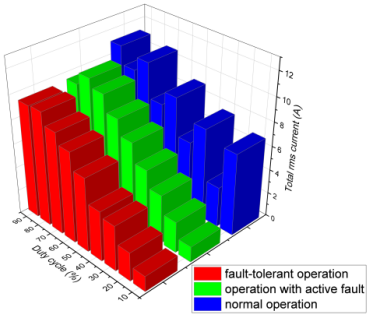
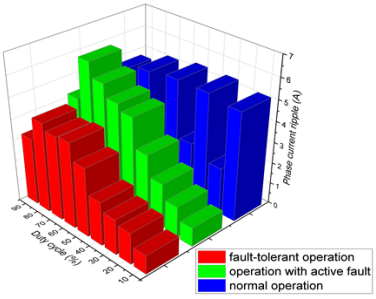


Figure 3.11. Comparison between a) phase current and b) total output current rms values in different operation modes

a)



b)

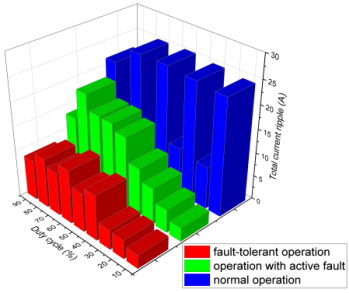


Figure 3.12. Comparison between a) phase current and b) total output current ripples in different operation modes

The current ripples in normal 5-phase operation mode reach maximums at duty cycle values of 10 %, 30 %, 50 %, 70 % and 90 %, but the minimums are observed at duty cycle values of 20 %, 40 %, 60 % and 80 %, as expected in a 5-phase converter with coupled inductors. The maximum and minimum current ripple values in normal operation mode have impact on the corresponding rms values. Therefore, phase and total current rms values represent the changes in ripples with a rising tendency when the duty cycle is increasing.

In case of operation with active fault, the current ripples and rms values are rising by increasing the duty cycle. The same tendency is observed in 4-phase fault-tolerant operation mode, however, the phase and total current rms values are lower in comparison with operation with active fault. The maximum phase current ripples and the total current ripple show a significant decrease by enabling the fault-tolerant operation algorithm in case of an active fault, especially in case of total current ripples. Hence, the proposed algorithm helps to reduce ripples and, sequentially, the current rms values, thus, improving efficiency in wide duty cycle range.

Finally, the converter dynamic behaviour is analysed by evaluating the transitions between different modes of converter operation at nominal duty cycle. The phase currents during transition between 3 different modes of operation is shown in (Fig. 3.13) under circumstances of intentionally applied 2.5 ms delay for the fault-tolerance algorithm turn-on. The phase currents during an automatic transition to fault-tolerant operation right after the fault occurrence is shown for high and moderate load in (Fig. 3.14) and (Fig. 3.15), respectively.

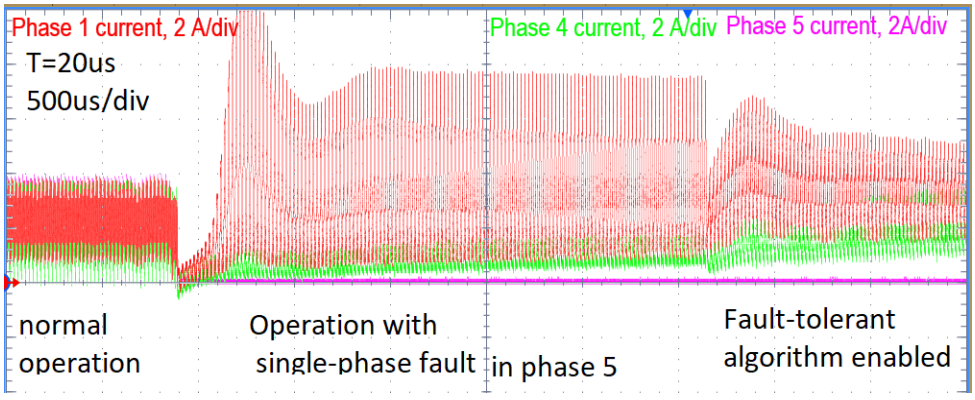


Figure 3.13. Phase currents during transition between normal operation, operation with single phase fault and fault-tolerant operation with additional delay

The transitions between different modes differs depending on converter load and transition type. As can be seen from the (Fig. 3.13), current transients with overshoots can be observed under high load conditions. The transient lasts approximately 1 ms before steady state is reached. Likewise in (Fig. 3.8), under high load conditions the phase currents show high peaks, caused by inductor partial saturation during 2.5 ms long operation with an active fault. Nevertheless, shortly after enabling the fault-tolerant operation the current peaks are reducing. In case of direct transition to fault-tolerant operation under high load the transient lasts approximately 600 µs and current ripples are kept at low level, as shown in (Fig. 3.14).

However, a short pulse transient with high current peak is observed at the initial stage of transition. An automatic transition to fault-tolerant operation under moderate load is running smoother. According to (Fig. 3.15), a slow transient and no overshoot is observed during transient. Moreover, the total current ripple is significantly reduced right after the fault occurrence and enabling the fault-tolerant operation algorithm.

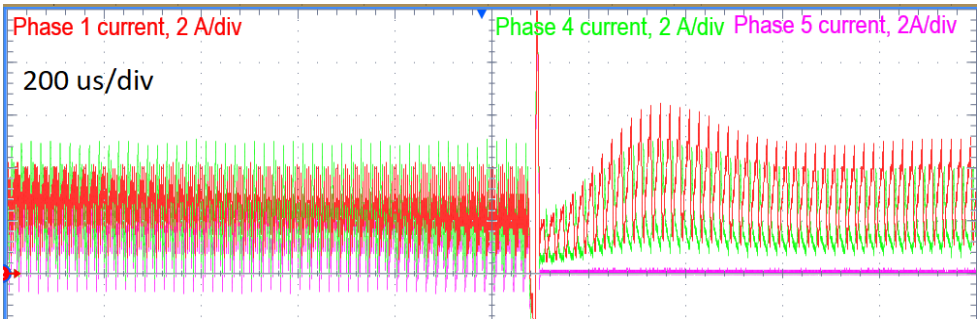


Figure 3.14. The phase currents during an automatic transition to fault-tolerant operation right after the fault occurrence under high load conditions

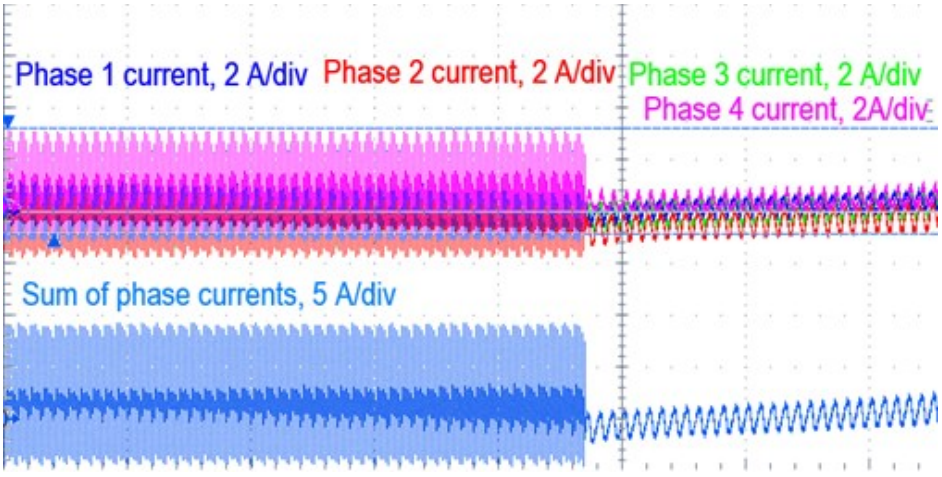


Figure 3.15. The phase currents during an automatic transition to fault-tolerant operation right after the fault occurrence under moderate load conditions

The transitions between different modes can be realized very fast. Right after the fault occurrence, an algorithm requires 1 or 2 switching periods to re-distribute the PWM carrier phase shifts and set-up the fault-tolerant operation mode. Practically, the transition lasts 20 to 40 μs, including fault detection and identification, but the acquired transition time slot is small enough to avoid any risks of converter damage. Hence, further converter operation with minor performance degradation is possible even with an active fault. However, care must be taken

during the output capacitance value estimation because the output capacitor must ensure voltage stability during transients [53].

3.3. Conclusions

The DC link current waveforms reflect the most common converter failure modes and the proposed ICM based technique can detect the overall fault condition and specify the failed component within 10 to 20 us in case of open circuit and less than 4 us in case of short circuit even in converter with strongly magnetically coupled inductors. The fault state detection and identification method show reliable performance within the whole converter duty cycle range, including transient operation and protection against pseudo-fault detection events.

The designed fault tolerant control system can avoid converter shutdown and provide an effective solution for converter operation with optimal performance in case of active semiconductor switch or inductor open circuit fault. The proposed algorithm has shown smaller current ripples and rms values, loss power reduction and efficiency improvements by up to 2 % in comparison with operation with active fault without fault-tolerant algorithm applied. In comparison with normal operation, the application of fault-tolerant operation algorithm results in minor efficiency decrease and ensures high performance especially under high load conditions. A fast transition to fault-tolerant algorithm is performed in case of fault occurrence and further converter operation with minor performance degradation.

4. ENERGY EFFICIENCY IN AUXILIARY CONVERTERS

Auxiliary converter system efficiency is the major key to achieve the objective of energetically and economically effective technology. The auxiliary systems must be provided with a reliable power supply that consumes minimum amount of energy for the specified purposes. This chapter discusses the potential of wide bandgap semiconductor use in auxiliary converters and analyses the further energy saving measures. A detailed analysis is shown in [2].

4.1. Wide bandgap semiconductor utilization in auxiliary converters

Wide bandgap (WGB) semiconductor devices have gained an increased interest within the last few decades in different fields and applications. While the WBG materials like Ge, GaAs, InP, ZnO and ZnS are less commonly used in power electronics, the silicon carbide (SiC) and gallium nitride (GaN) semiconductors are the most frequently mentioned and applied types of WGB devices that are currently spreading on the market [59]. In comparison with the classical silicon (Si), the SiC and GaN WBG semiconductors offer significantly lower switching losses and operation capabilities at considerably higher switching frequencies [59]-[65], resulting in choice of smaller passive filter components [63], better EMI performance and elimination of acoustic effects [60]. Furthermore, their ohmic conduction characteristics lead to reduced conduction losses at light loads [55], but combined with switching loss minimization, WBG semiconductors offer a potential for achieving very high efficiencies in typical power electronics applications [62]-[66].

SiC MOSFET devices have multiple considerable advantages in comparison with Si IGBTs. SiC shows higher breakdown electric field, wide energy bandgap of 3.23 eV, higher saturation velocity, thermal conductivity and melting point [59], thus, ensuring higher blocking voltage, switching frequency and withstanding thermal stresses with reduced heat sink volume. However, SiC electron mobility is considerably lower than by Si and GaN devices [59], therefore, in terms of switching frequency SiC has lower theoretical limits than GaN devices. As the result, the operational parameters of SiC semiconductors show significantly higher performance compared to Si [61]-[64], [66] but slightly poorer results than GaN [61]-[63]. Nevertheless, in comparison with GaN the price and availability on the market of SiC semiconductor devices is more competitive and is expected to approach the Si level in the next 5 years [59]. Hence, the SiC MOSFETs offer an attractive solution for power electronics converter design in typical inverter applications [60], [61] already nowadays, allowing to achieve high performance.

While the SiC MOSFETs are becoming to be widely implemented in different fields with higher voltage levels, the GaN devices are less common and still intended for use in specific low voltage power converters [67], [68]. Nevertheless, GaN shows the highest breakdown electric field and wide energy bandgap of 3.5 eV for ensuring potentially higher blocking voltage, the highest saturation velocity and electron mobility enabling operation with extremely high switching frequencies, but average thermal parameters like conductivity and melting point [59]. This results in potentially the best performance of GaN devices in comparison with Si and

SiC [61]-[63]. Despite that, GaN semiconductors nowadays have very tiny market share, still not available in voltage classes above 650 V, have lower reliability [59], [61] and, therefore, are challenging to be utilized in typical applications without transition to multilevel topologies [61], [66]. In the future GaN semiconductors are expected to show the highest market share growth [59] by reducing the price and improving reliability.

Application of WBG semiconductor devices in power electronics applications leads to considerable loss reduction and efficiency improvements. In [63] the Si IGBTs, SiC MOSFETs and GaN HEMTs have been evaluated in a T-type single phase inverter and shown enhancements in switching performance, efficiency rise, heat sink and output filter volume reduction with lower harmonic distortions by moving from Si to GaN semiconductor implementation, respectively. Considerable efficiency rise has been achieved by Si/SiC hybrid switch utilization in 3-level NPC inverter in [60]. In [65] the GaN potential of very high-power density is shown in different battery charging applications from 5 V 240 W up to 11 kW and 1 kV. While [67] and [23] has experimentally verified the GaN fast switching performance in low voltage applications, in [68] it is approved that GaN based inverter can be designed for operation under harsh cryogenic conditions, despite the reliability issues mentioned in [59]. Furthermore, studies [69]-[71] have verified that application of SiC MOSFETs in auxiliary converters in different types of railway application gives not only considerable loss reduction, but also leads to more compact design and reduced weight due to less powerful cooling system and, hence, reduces the overall vehicle energy consumption. Hence, it is reasonable to consider the implementation of WBG semiconductors in converters for transportation application.

WGB devices can lead to considerable benefits in auxiliary power supply design for different electric transportation applications. In [69] it has been shown that the SiC MOSFET use allows the lightweight converter design by reducing losses and heat sink volume, however, more careful busbar design is required to eliminate parasitic effects and achieve optimal switching performance. In [70] SiC devices ensure efficiency increase with reduced LC filter element volume reduction due to faster switching, resulting in higher auxiliary converter power density. Loss reduction correlated to SiC use has been shown also in [71], but even more considerable efficiency improvement was observed in combination with more advanced DC/DC converter design with optimized commutation loop [71]. Hence, implementation of WBG devices becomes especially advantageous in combination with the optimized auxiliary converter design.

For the experimental evaluation of SiC MOSFET and GaN FET performance, a prototype of 3-phase 3-level neutral point diode clamped inverter has been used (Fig. 1.13), (table 1.3). In the inverter prototype the 650 V class commercially available WBG transistors and SiC Schottky diodes are used. The selection of the transistors was based on the criteria of broad availability on market at the time of their purchase, while the new designs and obsolete components were excluded from selection. The case study system of the WBG device evaluation considers the following criteria:

- Efficiency and loss power distribution in wide operation range;
- Switching performance and ripples, including THD and EMI;
- Initial purchase costs and operational costs;

- Maintenance (reliability).

As the result, the analysed WBG semiconductor device utilization in electric transport auxiliary drives is assessed from different perspectives. For the WBG device performance evaluation the efficiency is assessed in different AC output frequency and switching frequency modes. Firstly, the measurements are performed with the SiC MOSFETs being installed. Secondly, the SiC MOSFETs are uninstalled and replaced by GaN FETs. Then the same measurements are repeated for correct data comparison. Efficiency η is calculated based on input and output power, according to (4.1). The input DC power is estimated by the external supply unit using input current and voltage by (4.2), but the AC power is measured using oscilloscope differential line voltages and phase currents probes with the 2-wattmeter method as in (4.3). Additionally, the prototype inverter loss distribution is evaluated using the thermal imager.

$$\eta = \frac{P_{out}}{P_{in}} \cdot 100\ \% \tag{4.1.}$$

where η – inverter efficiency, %;

P_{out} – output (AC) power, W;

P_{in} – input (DC) power, W.

$$P_{in} = V_{DC} \cdot I_{DC} \tag{4.2.}$$

where P_{in} – input (DC) power, W;

V_{DC} – input (DC) voltage, V;

I_{DC} – input (DC) current, A.

$$P_{out} = V_{UV} \cdot I_U + V_{WV} \cdot I_W \tag{4.3.}$$

where P_{out} – output (AC) power, W;

V_{UV} – line rms voltage (AC) between phases U and V, V;

V_{WV} – line rms voltage (AC) between phases W and V, V;

I_U – rms current (AC) in phase U, A;

I_W – rms current (AC) in phase W, A.

Driver parameters are adjusted for optimal switching performance in each case. The dead time circuit, gate impedance and snubber circuit passive components are being replaced, to obtain moderate switching transients and minimize losses, as well as to avoid parasitic turn-on events. The adjustable driver circuit elements are shown in (Fig. 4.1). The driver parameter adjustments have been performed for the optimal SiC and GaN FET switching performance in terms of voltage ringing effects, turn-on and turn-off times. The resultant driver parameters according to (Fig. 4.1) schematics are listed in (table 4.1).

Finally, for the economical aspect assessment, the semiconductor device costs are evaluated separately and in scope of the total system costs. Additionally, the reliability in field operation conditions and failure rates are discussed, as these factors will have considerable impact on the total life cycle costs. The efficiency and loss distribution results of SiC and GaN semiconductor operation are interpreted in conjunction with their potential application in auxiliary variable frequency drive systems for transportation application. Hence, the total WGB semiconductor performance evaluation will cover different aspects to draw the considered conclusions.

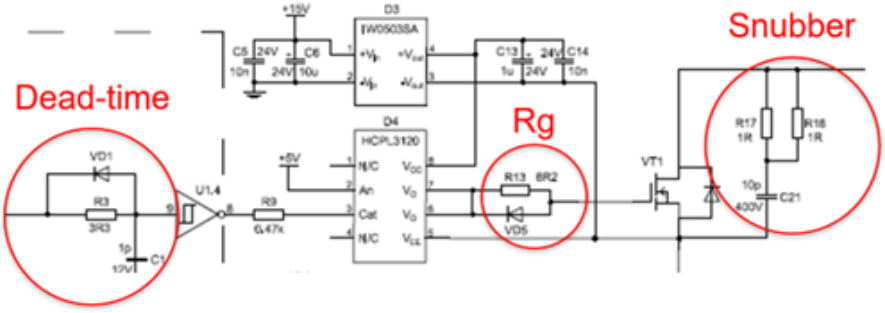


Figure 4.1. The adjustable driver circuit elements

Table 4.1.

Adjustable driver circuit element parameters

Parameters		Values	
Designator	Name	SiC MOSFETs	GaN FETs
C1	Dead-time circuit capacitance	10 pF	1 pF
R3	Dead-time turn on resistance	3.3 Ω	3.3 Ω
VD1	Dead-time turn off diode	1N4148	1N4148
Rg	Gate resistance configuration	R13 ‖ VD6	R13-L_g
R13	Gate resistance	10 Ω	27 Ω
L_g	Gate inductance	-	320 nH
VD6	Gate turn off diode	MBRA360T3	-
R16	Snubber resistancec	0.5 Ω	1 Ω
C21	Snubber capacitancec	10 pF	10 pF

The performance of SiC and GaN semiconductors in a 3-phase 3-level inverter is evaluated and compared with each other. The acquired line voltage and phase current waveforms with the output current frequency of 50 Hz and variable switching frequency of 1, 10 and 100 kHz, for inverter operation with SiC MOSFETs and GaN FETs is shown in (Fig. 4.2). The corresponding thermal images of loss power distribution with the output current frequency of 50 Hz and variable switching frequency of 1, 10 and 100 kHz for inverter operation with SiC MOSFETs and GaN FETs is shown in (Fig. 4.3). Inverter operation with both compared types of WBG semiconductor devices shows similar voltage and current waveforms. As the driver parameters have been adjusted for similar switching performance in terms of turn on and off times, and voltage ringing effects, the resultant line voltage and phase current waveforms are identical in both cases. With the increase in switching frequency, a significant reduction in current ripples is observed and in case of switching frequency of 100 kHz the current ripples are almost eliminated, resulting in lower THD and conduction losses. However, at higher switching frequency, the inverter efficiency decreases.

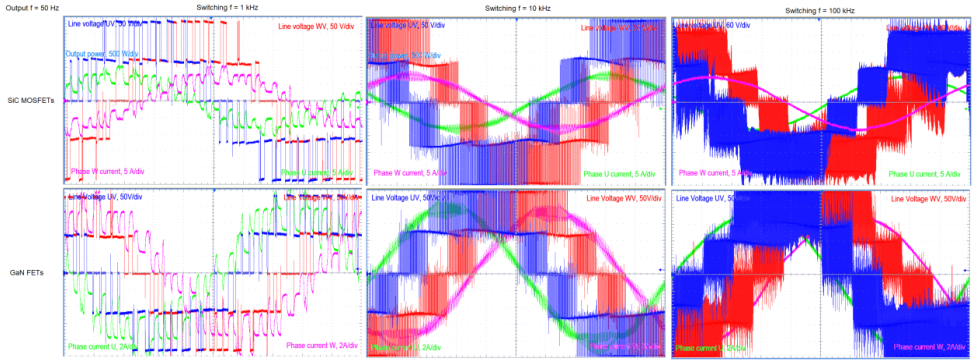


Figure 4.2. Line voltage and phase current waveforms with the output current frequency of 50 Hz and variable switching frequency of 1, 10 and 100 kHz, for inverter operation with SiC MOSFETs and GaN FETs

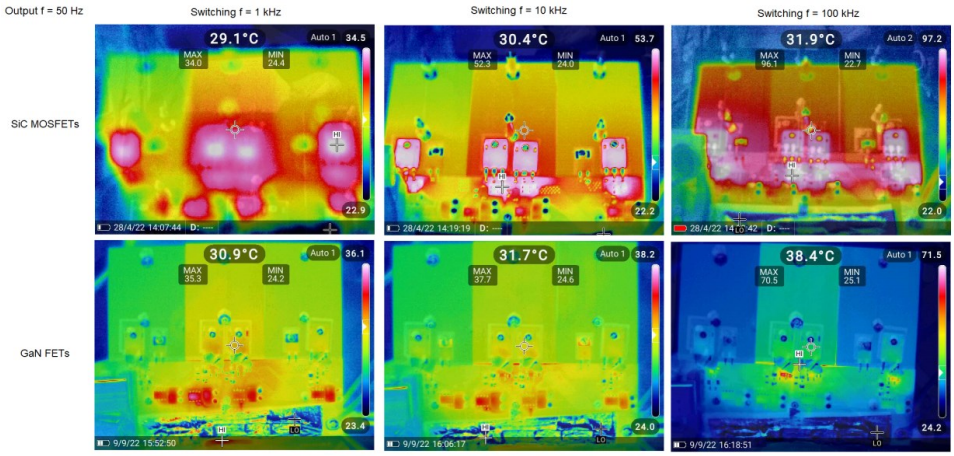
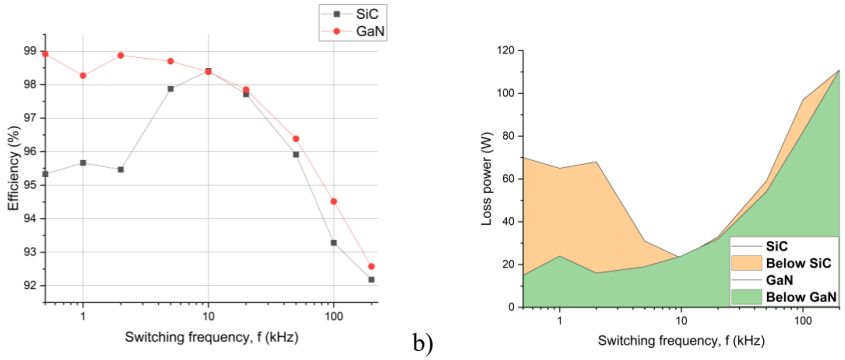


Figure 4.3. Thermal images of loss power distribution with the output current frequency of 50 Hz and variable switching frequency of 1, 10 and 100 kHz for inverter operation with SiC MOSFETs and GaN FETs

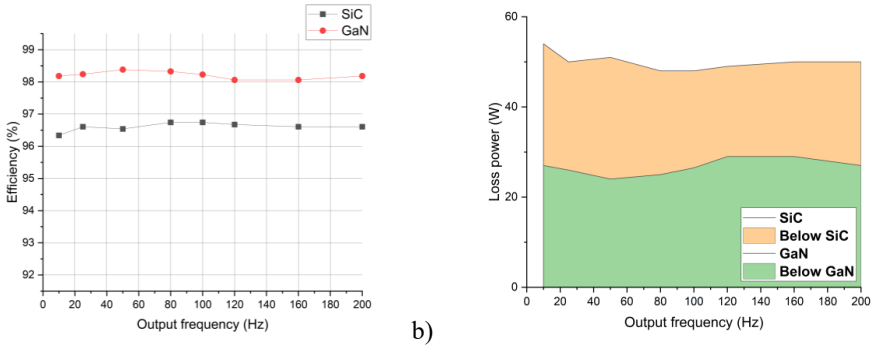
Inverter input and output power measurements have been performed in wide range of AC frequency and switching frequency for efficiency and loss power estimation. The inverter efficiency and loss power depending on the switching frequency is shown for operation with SiC and GaN semiconductors with AC frequency of 50 Hz in (Fig. 4.4). The inverter efficiency and loss power depending on the AC frequency at 10 kHz switching frequency is shown in (Fig. 4.5). Efficiency depending on the inverter switching frequency shows the maxima at approximately 10 kHz, where the balance between switching losses and current ripples is achieved in case of operation with SiC MOSFETs. When operated with GaN FETs, inverter shows higher efficiency even at low frequencies, resulted from more efficient conduction in

freewheeling operation. In contrast with SiC MOSFETs where the Schottky diode has forward voltage drop, the GaN FETs have pure resistive conduction losses if the gate-source voltage is set to high. Hence, the GaN FETs show more efficient conduction that has more considerable impact at light loads and low switching frequencies, where the conduction losses are dominant.



a) b)

Figure 4.4. Comparison between inverter a) efficiency and b) loss power, depending on the switching frequency for operation with SiC and GaN semiconductors



a) b)

Figure 4.5. Comparison between inverter a) efficiency and b) loss power, depending on the AC frequency for operation with SiC and GaN semiconductors

With higher switching frequencies the switching losses become dominant and that reduces the efficiency. Efficiency depending on the inverter output AC frequency shows the values between 98 and 99 % in wide range of operation with GaN FETs. In case of SiC MOSFETs, the inverter efficiency is lower by 1…1.5 %. Nevertheless, it must be mentioned that the SiC MOSFET driving circuit has been operated with the 15 V supply voltage, while the recommended gate-source voltage is 18 V to achieve maximum efficiency. Further analysis of the thermal imager data approves the power measurement results and shows an additional loss power source in the RC snubber circuits. The loss distribution shows considerable heat dissipation in snubber circuits, especially at high switching frequencies. Comparison of SiC and GaN operation in terms of heat dissipation from semiconductor devices is obviously showing

benefits of GaN FET operation, where the temperature of transistors is lower. Hence, the WBG semiconductor comparison results approve that GaN has lower losses and can achieve higher efficiencies.

Finally, the single semiconductor switch costs, total semiconductor costs and other component costs (i.e., PCB, passive components, integrated circuits, controller board etc...) are estimated for comparison between Si, SiC and GaN semiconductors and depicted in (Fig. 4.6). The initial purchase price of WBG semiconductor devices is very high. In comparison with GaN and SiC, a similar Si IGBT initial price is 71 % and 59 % lower, respectively. However, in terms of total system component price, the Si semiconductors are only 8 % and 5 % cheaper, than the GaN and SiC ones, respectively, but the difference in terms of overall system price would be insignificant. Although the economic influence of considerable loss reduction and efficiency increase within auxiliary converter life cycle is challenging to determine, it can be assumed, that the total life cycle costs are very likely to be reduced by utilization of WBG devices. Nevertheless, as discussed in [59], the GaN FETs still have reliability issues resulting in higher failure rate that can lead to additional unforeseen maintenance costs in field operation. Therefore, in terms of economical aspects the SiC MOSFETs are more likely to be recommended for auxiliary converters in transportation applications nowadays.

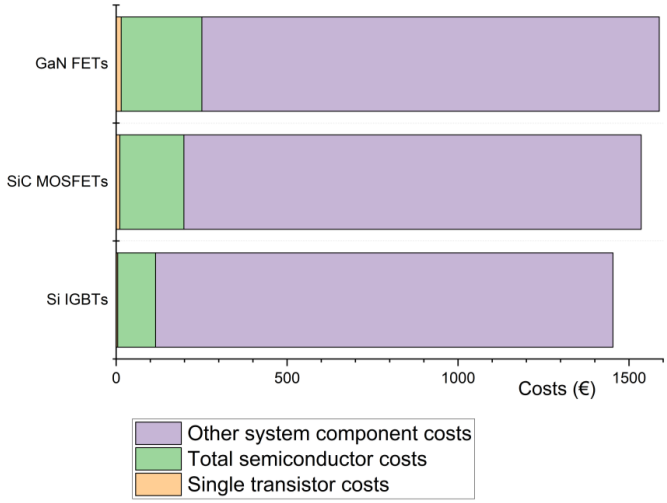


Figure 4.6. Comparison between Si, SiC and GaN single semiconductor switch costs, total semiconductor costs and other component costs

4.2. Variable frequency auxiliary drive

Auxiliary power demand in all types of vehicles has been gradually increasing within the last decades, caused by more safety and comfort systems being introduced, as well as the

electrification of auxiliary systems. As shown in [72], the operation of auxiliary systems has considerable impact on the overall vehicle energy consumption. The largest part of auxiliary power in vehicles make drive systems for heating, ventilation and air conditioning (HVAC), power steering unit (PSU) and air compressor, having power ratings ranging from 1 kW [72] up to 190 kVA [69]. Despite the significant technology advancements in power electronics and electrical drives, most of auxiliary systems in modern vehicles use conservative design approach with single auxiliary converter system producing 50 Hz AC supply for all systems simultaneously and induction machine (IM) – contactor system for each system drive [73]. Consequentially, the auxiliary drives are operating in cyclic load conditions with regular IM starting under load, nominal point operation and rest phases, resulting in high thermal and mechanical stresses and low efficiency of the system. Hence, a variable frequency drive concept operating with constant load can reduce the stresses and save energy. Moreover, the application of multi-level inverter topology to auxiliary drive can enhance the efficiency of the system [74]. Therefore, it is reasonable to investigate a novel auxiliary drive concept for application in electric transportation that ensures optimal efficiency and reliability for long life operation.

A case study on different auxiliary drive solutions is carried out on a vehicular air compressor example for comparative result assessment. Firstly, the performance of induction machine is compared between operation in nominal point with direct start versus variable frequency operation from the frequency converter. Secondly, the performance of permanent magnet synchronous machine (PMSM) is discussed in comparison with IM. In addition, an industrial frequency converter operation is compared with the supply from the GaN based 3-level NPC inverter. The initial data about the air compressor system and electrical drive parameters is obtained experimentally to build up the simulation model that is used for the case study comparative analysis. The compressed air consumption is modelled by a simplified mission profile repeating the city bus operation patterns in Jelgava, Latvia [75]. The data about the induction machine and frequency converter has been measured experimentally on the AEL-EEA and AEL-SERINCA laboratory testbenches from Edibon. An experimental setup and results are shown in (Fig. 4.7). The acquired data and system parameters have been combined in a multi-physical simulation model, shown in (Fig. 4.8).

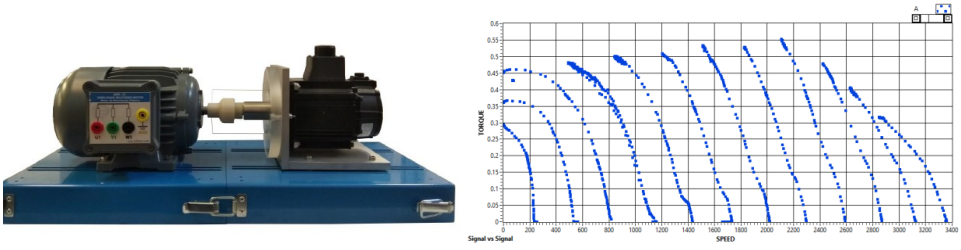


Figure 4.7. Induction machine data acquisition setup and results

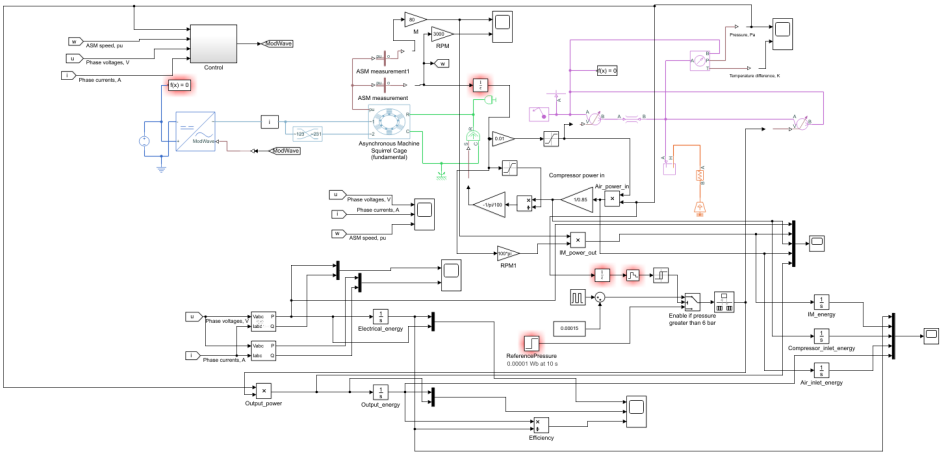
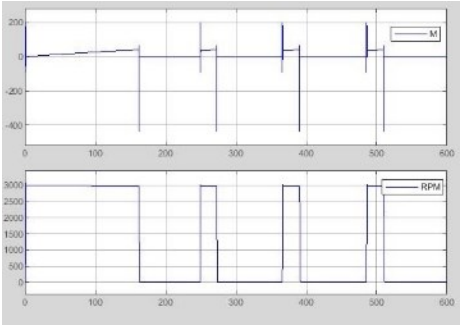


Figure 4.8. Simulation model for the case study

The induction machine torque and speed patterns for the system turn-on and further steady state operation in case of cyclic load and variable frequency operation are shown in (Fig. 4.9) a and b, respectively. The comparison between the pneumatic system air pressure patterns for cyclic and variable frequency operation are shown in (Fig. 4.10) a and b, respectively. The comparison between the system turn-on energy consumptions and steady state power are shown in (Fig. 4.11) a and b, respectively. Auxiliary drive for air compressor in variable frequency operation mode shows stable system pressure, gradual transitions between turn-on and steady state, energy consumption reduction by 2% at turn on and by 2.5% at steady state.

a) 

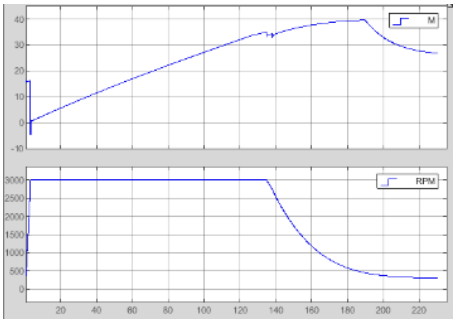
b) 

Figure 4.9. Induction machine torque and speed patterns for modes: a) cyclic, b) variable frequency

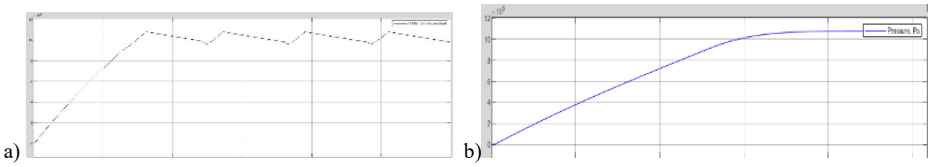


Figure 4.10. Pneumatic system air pressure patterns for modes a) cyclic, b) variable frequency

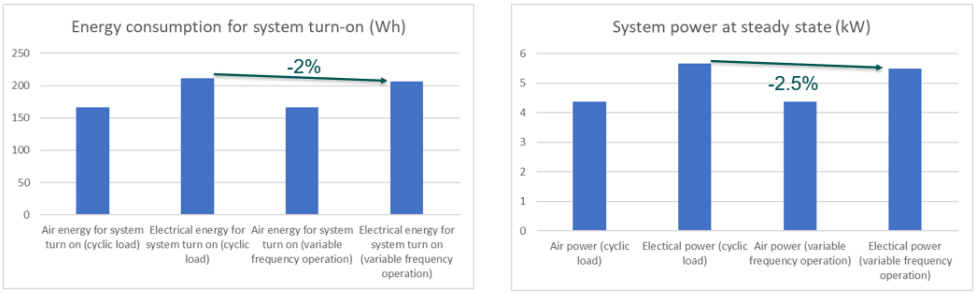


Figure 4.11. Comparison between operation modes a) energy consumption at turn-on, b) average power

Further energy savings are achieved by utilizing PMSM instead of IM, as well as by implementing GaN FETs in a 3-level NPC inverter topology that show efficiency about 99 % even at partial load [2]. The PMSM machine achieves better efficiency at partial load below the base speed, as there is no need for additional current for field weakening. In the case of IM, the operation at partial load below the base speed requires to generate additional current for maximum field creation that would be less effective solution in a partial load operation. In comparison with industrial frequency converter performing at average efficiency of 94 %, a 3-level NPC inverter performing at efficiency about 99 %. Hence, additional energy savings of about 1.5 % and 5 % can be achieved by utilizing PMSM instead of IM, as well as by implementing GaN FETs in a variable frequency inverter, respectively.

The pneumatic system air temperature patterns for in case of cyclic load and variable frequency operation are shown in (Fig. 4.12) a and b, respectively. The compressed air temperature is an effective indicator for the thermal stresses and additional energy waste. In case of variable frequency operation, after the system start-up, the air temperature is kept constant at low level. In contrast with cyclic load pattern, the compressed air temperature changes dramatically during all IM and compressor starts and turn-offs. Hence, on cyclic load operation, the thermal stress and mechanical stress due to frequent starts are high. By operating the system constantly with partial load thermal and mechanical stresses are minimized by reducing the component wear out due to frequent heavy starts and thermal stresses being reduced by 80 %. Moreover, keeping the compressed air temperatures at constant level can lead to additional energy savings of approximately 1 %. Hence, a variable frequency drive concept can reduce the stresses and save energy of the system.

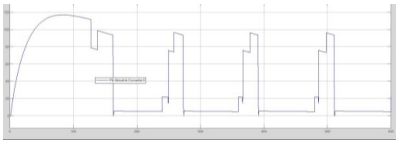
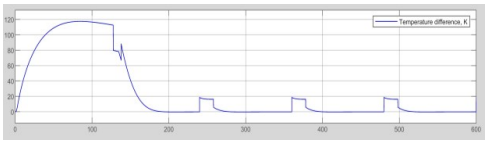
a)  b) 

Figure 4.12. Compressed air temperature patterns for modes a) cyclic, b) variable frequency

The proposed auxiliary drive concept ensures the highest efficiency in operation with partial load, light and balanced loading without heavy starts, significantly reduced wear out of components and energy savings by about 2.5 %. By utilizing PMSM drive with GaN FET NPC inverter the total efficiency improvement is estimated to reach about 10 %. Moreover, by operating the system in variable frequency mode, the thermal and mechanical stresses are minimized. As a result, the auxiliary drive system can be designed with downsized components, at the same time achieving more reliable field operation with an increased lifetime.

4.3. Conclusions

Auxiliary converter systems in transportation applications require novel solutions and designs to meet the rising auxiliary power demands. The proposed auxiliary inverter operation in variable frequency drive system shows high efficiency in wide range, therefore it has large potential for energy savings in a vehicular auxiliary system, i.e., air compressor, steering power unit and air conditioning system. The 3-level inverter topology allows utilization of semiconductors with lower breakdown voltage, minimizes the current ripples, THD and EMI, as well as offering more efficient operation with reduced switching losses. In combination with the WBG semiconductor use, the proposed 3-level inverter in variable frequency operation has even more benefits in terms of loss minimization in full operational range of auxiliary drives, especially by enabling considerably more efficient operation at light loads and at reduced voltage.

Wide bandgap semiconductors have shown excellent performance with efficiencies above 96 % in typical auxiliary converter operation modes. Utilization of GaN semiconductors in a 3-phase 3-level inverter for auxiliary variable frequency drive application results in the maximum efficiency in all operating modes, however, it has the highest initial purchase costs and possibility of failure leading to risks of higher total life cycle costs due to possibility of additional maintenance in the field operation. In comparison with Si, a high initial price for SiC devices is likely to be compensated by the considerable loss reduction and reliable field operation. Therefore, the use of auxiliary converters utilizing SiC semiconductors in transportation applications is currently more advisable, as the inverter design with SiC MOSFETs and Schottky diodes is nowadays still technically and economically more effective.

The proposed auxiliary drive concept in combination with the PMSM drive with GaN FET NPC inverter shows the highest efficiency in operation with partial load, light and balanced

loading without heavy starts, significantly reduced wear out of components, thermal stress reduction by 80 % and energy savings by about 10 %. By operating the system in variable frequency mode, the thermal and mechanical stresses are minimized, resulting in downsized components, at the same time achieving more reliable field operation with an increased lifetime.

CONCLUSIONS

Electric vehicles require volume- and cost-effective, efficient and modular auxiliary converter system design. By introducing a set of technological advancements discussed in this Thesis, the aim of designing an energetically and economically effective technology for auxiliary converter systems in electric vehicles can be fulfilled. The total energy savings by auxiliaries can reach up to 10 % with stress reduction by up to 80 % and considerable functionality improvements in reliability and fault tolerance.

The novel indirect current measurement (ICM) technique allows to achieve a cost-efficient auxiliary converter sensing and measurement design with functionality of the current sensing and balancing; fault detection and identification; as well as the fault-tolerant operation.

The ICM implementation in a multi-phase DC converter has shown adequate accuracy for current balancing with measurement errors below 0.5 A resulting in no efficiency degradation, fast fault detection and identification capability within 1 converter switching period or 20 μs and efficient fault-tolerant operation that can allow converter operation with active fault condition and improve efficiency by up to 2 %. The proposed ICM technique implementation in combination with intelligent control system is considered as a key technology for the converter high efficiency, optimized performance, fault tolerance and reliable power supply for safety critical systems.

Wide bandgap semiconductor utilization in combination with ICM results in significantly higher efficiency and reduced volume that allows to achieve higher auxiliary converter power density level, faster operation, and power loss reduction by up to 5 %. Moreover, the application of the wide bandgap devices is technically and economically effective.

Use of variable frequency drive concept in vehicular auxiliary systems with wide bandgap device-based multi-level inverter has shown low total harmonic distortion and electromagnetic interference levels with high efficiency in wide operation range that results in energy savings of approximately 10 %, longer lifetime and more reliable operation with thermal stresses being reduced by 80 %.

In scope of the future research, the ICM concept can be extended for other multi-phase and multi-level auxiliary converter topologies, utilizing wide bandgap semiconductors to propose a solution for the complete auxiliary system modernization. The achieved results have a strong potential for commercialization and can be further developed for the testing in the application relevant environment, certification, type approval and release to the market within the next 4 years.

REFERENCES

[1] P. Hołyszko, D. Zieliński, A. Niewczas, J. Rymarz, and E. Dębicka, “Ensuring the Continuity of Power Supply to the On-Board Auxiliary Devices of the Trolleybus through the Recuperation of Kinetic Energy,” *Energies*, vol. 14, no. 16, p. 5035, Aug. 2021, doi: 10.3390/en14165035.

[2] A. Bogdanovs, O. Krievs and J. Pforr, “Wide Bandgap SiC and GaN Semiconductor Performance Evaluation in a 3-Phase 3-Level NPC Inverter for Transportation Application,” *2022 IEEE 63th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, 2022, pp. 1-7, doi: 10.1109/RTUCON56726.2022.9978767.

[3] Kondratieva, L., Bogdanovs, A., Overianova, L., Riabov, I., Goolak, S. “Determination of the Working Energy Capacity of the On-Board Energy Storage System of an Electric Locomotive for Quarry Railway Transport during Working with a Limitation of Consumed Power,” *Archives of Transport*, vol. 65, no. 1, pp. 119-136, doi:10.5604/01.3001.0016.2631

[4] S. He et al., "Digital Collaborative Development of a High Reliable Auxiliary Electric Drive System for eTransportation: From Dual Three-Phase PMSM to Control Algorithm," in *IEEE Access*, vol. 8, pp. 178755-178769, 2020, doi: 10.1109/ACCESS.2020.3027633.

[5] T. M. Jahns and B. Sarlioglu, "The Incredible Shrinking Motor Drive: Accelerating the Transition to Integrated Motor Drives," in *IEEE Power Electronics Magazine*, vol. 7, no. 3, pp. 18-27, Sept. 2020, doi: 10.1109/MPEL.2020.3011275.

[6] D. Cittanti, E. Vico, E. Armando and R. Bojoi, "Analysis and Conceptualization of a 400V 100 kVA Full-GaN Double Bridge Inverter for Next-Generation Electric Vehicle Drives," *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, Anaheim, CA, USA, 2022, pp. 740-747, doi: 10.1109/ITEC53557.2022.9813847.

[7] S. Utz and J. Pforr, "Turn-on behavior of automotive multi-phase converters with coupled inductors," *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Novi Sad, Serbia, 2012, pp. LS3c.3-1-LS3c.3-8, doi: 10.1109/EPEPEMC.2012.6397434.

[8] S. Utz and J. Pforr, "Impact of input and output voltage perturbation on the behavior of automotive multi-phase converters with coupled inductors," *2011 IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, USA, 2011, pp. 4169-4176, doi: 10.1109/ECCE.2011.6064337.

[9] J. Czogalla, Jieli Li and C. R. Sullivan, "Automotive application of multi-phase coupled-inductor DC-DC converter," *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference*, 2003., Salt Lake City, UT, USA, 2003, pp. 1524-1529 vol.3, doi: 10.1109/IAS.2003.1257758.

[10] S. Utz and J. Pforr, "Current-balancing controller requirements of automotive multi-phase converters with coupled inductors," *2012 IEEE Energy Conversion Congress and*

Exposition (ECCE), Raleigh, NC, USA, 2012, pp. 372-379, doi: 10.1109/ECCE.2012.6342798.

[11] H. Kim, M. Falahi, T. M. Jahns and M. W. Degner, "Inductor Current Measurement and Regulation Using a Single DC Link Current Sensor for Interleaved DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1503-1510, May 2011, doi: 10.1109/TPEL.2010.2084108.

[12] J. C. Schroeder, M. Petersen and F. W. Fuchs, "One-sensor current sharing in multiphase interleaved DC/DC converters with coupled inductors," *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Novi Sad, Serbia, 2012, pp. DS3c.1-1-DS3c.1-7, doi: 10.1109/EPEPEMC.2012.6397338.

[13] Y. -H. Cho, A. Koran, H. Miwa, B. York and J. -S. Lai, "An active current reconstruction and balancing strategy with DC-link current sensing for a multi-phase coupled-inductor converter," *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, USA, 2010, pp. 3414-3419, doi: 10.1109/ECCE.2010.5618316.

[14] S. Mariethoz, A. G. Beccuti and M. Morari, "Model predictive control of multiphase interleaved DC-DC converters with sensorless current limitation and power balance," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, Greece, 2008, pp. 1069-1074, doi: 10.1109/PESC.2008.4592071.

[15] J. Gordillo and C. Aguilar, "A Simple Sensorless Current Sharing Technique for Multiphase DC–DC Buck Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3480-3489, May 2017, doi: 10.1109/TPEL.2016.2592240.

[16] K. -Y. Hu, Y. -S. Chen and C. -H. Tsai, "A Digital Multiphase Converter with Sensorless Current and Thermal Balance Mechanism," *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Tainan, Taiwan, 2018, pp. 175-178, doi: 10.1109/ASSCC.2018.8579301.

[17] J. Han and J. -H. Song, "Phase Current-Balance Control Using DC-Link Current Sensor for Multiphase Converters With Discontinuous Current Mode Considered," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4020-4030, July 2016, doi: 10.1109/TIE.2016.2530781.

[18] H. -C. Chen, C. -Y. Lu and C. -H. Lu, "Control of Bidirectional Interleaved DC-DC Converter With Single Current Sensor," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018, pp. 2171-2177, doi: 10.1109/ECCE.2018.8557828.

[19] H. -C. Chen, C. -Y. Lu and L. -M. Huang, "Decoupled Current-Balancing Control With Single-Sensor Sampling-Current Strategy For Two-Phase Interleaved Boost-Type Converters," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 3, pp. 1507-1518, March 2016, doi: 10.1109/TIE.2015.2498135.

[20] R. P. Singh and A. M. Khambadkone, "Current Sharing and Sensing in N-Paralleled Converters Using Single Current Sensor," in *IEEE Transactions on Industry Applications*, vol. 46, no. 3, pp. 1212-1219, May-june 2010, doi: 10.1109/TIA.2010.2045333.

[21] M. Stadler and J. Pforr, "Multi-phase Converter for Wide Range of Input Voltages with Integrated Filter Inductor," *2006 12th International Power Electronics and Motion Control Conference*, Portoroz, Slovenia, 2006, pp. 106-111, doi: 10.1109/EPEPEMC.2006.4778384.

[22] V. Yousefzadeh and S. Choudhury, "Nonlinear digital PID controller for DC-DC converters," *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Austin, TX, USA, 2008, pp. 1704-1709, doi: 10.1109/APEC.2008.4522956.

[23] K. Kroics, "Design of Interleaved GaN Transistor Based Buck Converter with Directly Coupled Foil Winding Inductor," CIPS 2020; *11th International Conference on Integrated Power Electronics Systems*, Berlin, Germany, 2020, pp. 1-6.

[24] K. Kroics, J. Zakis and U. Sirmelis, "Multiphase interleaved DC-DC converter with directly and inversely coupled inductors," *2016 57th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, 2016, pp. 1-6, doi: 10.1109/RTUCON.2016.7763102.

[25] A. Bogdanovs, O. Krievs and J. Pforr, "Indirect DC link current measurement technique using an op-amp circuit in an automotive DC converter with coupled inductors," *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Germany, 2020, pp. 1-8.

[26] S. Kim, J. -I. Ha and S. -K. Sul, "Single shunt current sensing technique in three-level PWM inverter," *8th International Conference on Power Electronics - ECCE Asia*, Jeju, Korea (South), 2011, pp. 1445-1451, doi: 10.1109/ICPE.2011.5944454.

[27] H. Shin and J. -I. Ha, "Phase Current Reconstructions from DC-Link Currents in Three-Phase Three-Level PWM Inverters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 582-593, Feb. 2014, doi: 10.1109/TPEL.2013.2257866.

[28] X. Li, S. Dusmez, B. Akin and K. Rajashekara, "A new SVPWM for phase currents reconstruction of three-phase three-level T-type converters," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA, 2015, pp. 1582-1588, doi: 10.1109/APEC.2015.7104558.

[29] X. Li, S. Dusmez, B. Akin and K. Rajashekara, "A New SVPWM for the Phase Current Reconstruction of Three-Phase Three-level T-type Converters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2627-2637, March 2016, doi: 10.1109/TPEL.2015.2440421.

[30] Y. Son and J. Kim, "A Novel Phase Current Reconstruction Method for a Three-Level Neutral Point Clamped Inverter (NPCI) with a Neutral Shunt Resistor," *Energies*, vol. 11, no. 10, p. 2616, Oct. 2018, doi: 10.3390/en11102616.

[31] J. -J. You, J. -H. Jung, C. -H. Park and J. -M. Kim, "Phase current reconstruction of three-level Neutral-Point-Clamped(NPC) inverter with a neutral shunt resistor," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, 2017, pp. 2598-2604, doi: 10.1109/APEC.2017.7931064.

[32] A. Suzdalenko, J. Zakis and O. Krievs, "Single-loop Current Sensorless Control with Self-detection of Conduction Losses Applied to Neutral Point Clamped Multilevel Converter," *2019 11th International Conference on Electrical and Electronics Engineering (ELECO)*, Bursa, Turkey, 2019, pp. 250-254, doi: 10.23919/ELECO47770.2019.8990464.

[33] F. Blaabjerg, J. K. Pedersen, U. Jaeger and P. Thoegersen, "Single current sensor technique in the DC link of three-phase PWM-VS inverters: a review and a novel solution," in *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1241-1253, Sept.-Oct. 1997, doi: 10.1109/28.633802.

[34] Green, T.C.; Williams, B.W.: "Derivation of motor line-current waveforms from the DC-link current of an inverter", *IEE Proceedings B (Electric Power Applications)*, 1989, 136, (4), p. 196-204, DOI: 10.1049/ip-b.1989.0026.

[35] Lu Haifeng, Sheng Shuang, Guo Ruijie, Qu Wenlong and Wu Lixun, "Phase current sensor fault-tolerant technique using information of DC side current in two-level inverter," *2013 International Conference on Electrical Machines and Systems (ICEMS)*, Busan, 2013, pp. 1648-1651, doi: 10.1109/ICEMS.2013.6713324.

[36] A. Bogdanovs, O. Krievs and J. Pforr, "Indirect Multiple DC Link Current Sensing Using Op-Amp Circuits in a Three-Phase Three-Level PWM Inverter," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Online, 2021, pp. 1-8.

[37] A. Bogdanovs, O. Krievs, L. Ribickis and J. Pforr, "Fuzzy Logic Current Balancing Controller Implementation in an Automotive Multi-Phase DC Converter with Coupled Inductors," *2020 IEEE 61th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, 2020, pp. 1-10, doi: 10.1109/RTUCON51174.2020.9316473.

[38] O. Krievs and L. Ribickis, "Application of Fuzzy Logic Controllers in Industrial Electronics and Electrical Drives," *Power and Electrical Engineering*, Vol.5, 2002, pp.77-85, ISSN 1407-7345.

[39] L. J. Álvarez et al., "Design, analysis and modeling of an optimized fuzzy control algorithm for synchronous multiphase DC-DC converters in automotive applications," *2006 37th IEEE Power Electronics Specialists Conference*, Jeju, Korea (South), 2006, pp. 1-6, doi: 10.1109/pesc.2006.1712047.

[40] C. Dhanalakshmi, A. Saravanan, and R. Jeba Raj, "Current Balancing in Multiphase Converter Based on Interleaving Technique using Fuzzy Logic," *International Journal of Engineering Sciences & Research Technology*, vol.4, 2015, pp.80-89.

[41] X. Cui, W. Shen, Y. Zhang, and C. Hu, "A Fast Multi-Switched Inductor Balancing System Based on a Fuzzy Logic Controller for Lithium-Ion Battery Packs in Electric Vehicles," *Energies*, vol. 10, no. 7, p. 1034, Jul. 2017, doi: 10.3390/en10071034.

[42] M. Murken and P. Gratzfeld, "Reliability Comparison of Bidirectional Automotive DC/DC Converters," *2017 IEEE 86th Vehicular Technology Conference (VTC-Fall)*, 2017, pp. 1-7, doi: 10.1109/VTCFall.2017.8288329.

[43] W. May and J. Pforr, "Design of integrated inductors in multi-phase buck/boost converters including operation with deactivated phases," *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2019, pp. 1-8.

[44] S. Utz and J. Pforr, "Operation of multi-phase converters with coupled inductors at reduced numbers of phases," *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Birmingham, UK, 2011, pp. 1-10.

[45] A. Bogdanovs, O. Krievs and J. Pforr, "Fault Detection using Indirect DC Link Current Measurement Technique in Multiphase DC Converter with Coupled Inductor," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. P.1-P.10, doi: 10.23919/EPE21ECCEEurope50061.2021.9570190.

[46] A. Bogdanovs, O. Krievs and J. Pforr, "Fault-Tolerant Operation Algorithm for a Multi-Phase DC Converter with Coupled Inductors," *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg*, Germany, 2022, pp. 1-10, doi: 10.30420/565822070.

[47] K. Ma, H. Wang and F. Blaabjerg, "New Approaches to Reliability Assessment: Using physics-of-failure for prediction and design in power electronics systems," in *IEEE Power Electronics Magazine*, vol. 3, no. 4, pp. 28-41, Dec. 2016, doi: 10.1109/MPEL.2016.2615277.

[48] H. Wang and F. Blaabjerg, "Power Electronics Reliability: State of the Art and Outlook," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6476-6493, Dec. 2021, doi: 10.1109/JESTPE.2020.3037161.

[49] F. Blaabjerg, H. Wang, I. Vernica, B. Liu and P. Davari, "Reliability of Power Electronic Systems for EV/HEV Applications," in *Proceedings of the IEEE*, vol. 109, no. 6, pp. 1060-1076, June 2021, doi: 10.1109/JPROC.2020.3031041.

[50] J. Schuderer et al., "Health Management of Power Electronics Systems," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 948-955

[51] M. Ashourloo et al., "An Automotive-Grade Monolithic Masterless Fault-Tolerant Hybrid Dickson DC–DC Converter for 48-V Multi-Phase Applications," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3608-3618, Dec. 2021, doi: 10.1109/JSSC.2021.3105358.

[52] G. Selvaraj, A. R. Sadat, H. S. Krishnamoorthy and K. Rajashekara, "An Improved Fault-Tolerant Power Converter for Electric Vehicle Propulsion," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020, pp. 1-5, doi: 10.1109/PESGRE45664.2020.9070596.

[53] S. Siouane, S. Jovanović and P. Poure, "Open-Switch Fault-Tolerant Operation of a Two-Stage Buck/Buck–Boost Converter With Redundant Synchronous Switch for PV Systems," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3938-3947, May 2019, doi: 10.1109/TIE.2018.2847653.

[54] S. Kumar and B. S. Rajpurohit, "A Novel Fault Tolerant Control Scheme for Power Converter," *2020 IEEE International Power and Renewable Energy Conference*, 2020, pp. 1-5, doi: 10.1109/IPRECON49514.2020.9315247.

[55] E. Pazouki, J. A. De Abreu-Garcia and Y. Sozer, "A Novel Fault-Tolerant Control Method for Interleaved DC–DC Converters Under Switch Fault Condition," in *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 519-526, Jan.-Feb. 2020, doi: 10.1109/TIA.2019.2953030.

[56] M. M. Hillesheim, M. Cousineau and L. Hureau, "Reconfigurable Partial-Decentralized Control of a Multiphase Converter for Fail-Operational Automotive Processor Power Supply," *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1-P.8, doi: 10.23919/EPE.2019.8915561.

[57] M. Gleissner and M. Bakran, "Influence of inverse coupled inductors on fault-tolerant operation of two-phase DC-DC converters," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-11, doi: 10.1109/EPE.2015.7309059.

[58] S. Utz, M. Stadler and J. Pforr, "ACTIVE phase-shift control of multi-phase converters to minimize input current sub-harmonics," *2009 13th European Conference on Power Electronics and Applications*, Barcelona, Spain, 2009, pp. 1-10.

[59] G. Iannaccone, C. Sbrana, I. Morelli and S. Strangio, "Power Electronics Based on Wide-Bandgap Semiconductors: Opportunities and Challenges," in *IEEE Access*, vol. 9, pp. 139446-139456, 2021, doi: 10.1109/ACCESS.2021.3118897.

[60] J. W. Kolar and J. Huber, "Next-Generation SiC/GaN Three-Phase Variable-Speed Drive Inverter Concepts," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1-5.

[61] J. W. Kolar et al., "Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"," *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 27.7.1-27.7.4, doi: 10.1109/IEDM13553.2020.9372022.

[62] E. Shelton et al., "Fast Switching of High Current WBG Power Devices," *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022, pp. 1-8, doi: 10.30420/565822136.

[63] E. Gurpinar and A. Castellazzi, "Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs," in *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7148-7160, Oct. 2016, doi: 10.1109/TPEL.2015.2506400.

[64] H. Liu, T. Zhao and X. Wu, "Performance Evaluation of Si/SiC Hybrid Switch-Based Three-Level Active Neutral-Point-Clamped Inverter," in *IEEE Open Journal of Industry Applications*, vol. 3, pp. 90-103, 2022, doi: 10.1109/OJIA.2022.3179225.

[65] M. J. Kasper, J. A. Anderson, G. Deboy, Y. Li, M. Haider and J. W. Kolar, "Next Generation GaN-based Architectures: From 240W USB-C Adapters to 11kW EV On-

Board Chargers with Ultra-high Power Density and Wide Output Voltage Range," *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022, pp. 1-10, doi: 10.30420/565822004.

[66] J. Azurza Anderson, G. Zulauf, J. W. Kolar and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," in *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322-338, 2020, doi: 10.1109/OJPEL.2020.3018220.

[67] K. Kroics, "WBG semiconductors, interleaving and integration of magnetics for non-isolated DC-DC converter performance improvement," *2020 XI National Conference with International Participation (ELECTRONICA)*, Sofia, Bulgaria, 2020, pp. 1-7, doi: 10.1109/ELECTRONICA50406.2020.9305134.

[68] Mustafeez-ul-Hassan, A. I. Emon, F. Luo and V. Solovyov, "Design and Validation of a 20 kVA, Fully Cryogenic, 2-Level GaN Based Current Source Inverter for Full Electric Aircrafts," in *IEEE Transactions on Transportation Electrification*, doi: 10.1109/TTE.2022.3176842.

[69] I. -S. Lee, J. -Y. Kang, J. Lee and S. -T. Lee, "Design Considerations of Auxiliary Power Supply Unit with SiC MOSFET for Lightweight Railway Vehicles," *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, 2018, pp. 908-915, doi: 10.23919/ICEMS.2018.8549234.

[70] D. Wu, C. Xiao, H. Zhang and W. Liang, "Development of auxiliary converter based on 1700V/325A full SiC MOSFET for urban rail transit vehicles," *2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, 2017, pp. 1-6, doi: 10.1109/ITEC-AP.2017.8080769.

[71] M. -A. Ocklenburg, M. Döhmen, X. -Q. Wu and M. Helsper, "Next generation DC-DC converters for Auxiliary Power Supplies with SiC MOSFETs," *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1-6, doi: 10.1109/ESARS-ITEC.2018.8607463

[72] I. Evtimov, R. Ivanov, and M. Sapundjiev, “Energy consumption of auxiliary systems of electric cars,” in *MATEC Web Conf*., 2017, vol. 133, pp 1-5.

[73] Z. Biel, M. Šuňal and P. Kulha, "Application of inverter parallel operation strategy in railway auxiliary converters," *2022 International Conference on Applied Electronics (AE)*, Pilsen, Czech Republic, 2022, pp. 1-4.

[74] A. Sheir, M. Z. Youssef and M. Orabi, "A Novel Auxiliary Modular Inverter with Battery Integration for Electric Vehicle Applications," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 1730-1737, doi: 10.1109/APEC.2019.8721803.

[75] O. Sliskis, I. Dvornikovs, M. Marinbahs, J. Marks and E. Groza, "Investigation of electrical bus traction motor dynamic using methods of physical and computer simulation," *2019 16th Conference on Electrical Machines, Drives and Power Systems (ELMA)*, Varna, Bulgaria, 2019, pp. 1-4, doi: 10.1109/ELMA.2019.8771668.

Artūrs Bogdanovs was born in 1989 in Riga. He received a Bachelor's degree in Automotive Engineering from Riga Technical University (Latvia) in 2014 and a Master's degree in Automotive Engineering from the University of Applied Sciences Ingolstadt (Germany) in 2017. He has worked as a power electronics engineer at Riga Electric Machine Building Factory. Since 2020 he has worked at Riga Technical University, where he currently is a researcher and a lecturer. His research interests include DC converters, auxiliary power supplies, automotive power electronics, control engineering, e-mobility, and engineering education.